CMC Model Updates – November 2026

Planar SOI Transistor Models

Developed by UC Berkley

BSIM-SOI 4.7.1

Developed by UC Berkeley

Enhancements:

- 2026enh1 (ADI): Implement scaling rule as per section 10 of VerilogA Code Standards Version 1.3.0.

Bug fixes:

- 2025bug3 (Synopsys): BSIM-SOI 4.7.0 GMIN stamping issue.
- 2025bug4 (ADI): BSIM-SOI 4.7.0 non-ascii character removal from line 2245 of bsimsoi.va.
- 2026bug1 (UCB/IITK): Vampyre warning indicates that several model parameters are being subjected to geometry scaling while also having restricted ranges (0:∞).
- 2026bug2 (Cadence): Diffusion component of diode current is not linearized for higher Vd.
- 2026bug3 (UCB/IITK): Update qaSpec file to include tests for non-default values of parameters in QA suite.
- 2026bug4 (UCB/IITK): Update the MULT_I implementation in TNOIMOD = 3 to be consistent with the MULT-factor guidelines.

BSIM-SOI 100.1.2

Developed by UC Berkeley

Enhancements:

- 2026enh1 (ADI): Implementing scaling rule as per section 10 of VerilogA Code Standards Version 1.3.0.

Bug fixes:

- 2025bug7 (ADI/Siemens): Correction in BODYMOD definitions and related body current calculations.
- 2025bug8 (ADI): Removal of VAMPyRE errors/notices regarding model parameter definitions.
- 2026bug2 (Cadence): Removing redundant check on BODYMOD for warning statement regarding floating-body devices with fifth terminal as thermal node.
- 2026bug5 (Synopsys): Correcting the floating-body calculation for BODYMOD=0 and TNODEOUT=1 while the 5th terminal 'b' is a 'thermal' node.
- 2026bug7 (UCB/IITK): Updated the QA tests to cover both body contacted and floating body cases.

BSIM-SOI 101.0.0

Developed by UC Berkeley

Enhancements:

- 2023enh4 (GF): Improved mobility model for Vb dependency in SOIMOD=1.
- 2023enh5 (GF): Improved SS and mobility degradation fitting flexibility for SS in SOIMOD=1 for varied Vb.
- 2023enh6 (GF): Improved gm fitting in saturation by eliminating unwanted humps in PD to FD transition in SOIMOD=1.
- 2023enh7 (GF): Added low-frequency noise model of Diodes for floating-body effect.
- 2023enh8 (GF): Implementation of MULT_I, MULT_Q and MULT_FN.
- 2024enh1(GF): Addition of decoupled CVMOD (CVMOD=1 for SOIMOD=1).
- 2024enh2-3(UCB/GF): Removal of redundant “if-condition” in PD-FD initial guess formulation.
- 2026enh1 (ADI): Implement scaling rule as per section 10 of VerilogA Code Standards Version 1.3.0.

Bug fixes:

- 2025bug4 (UCB/IITK): Additional QA Tests for SOIMOD=1 with CVMOD=1 and GMCMOD=1.
- 2025bug5 (UCB/IITK): Issue with approximations related to small x_ds calculations, leading to AC Flip Test error.

- 2025bug6 (GF): Decoupling of EVB and ECB normalization parameters by introducing VEVB parameter.
- 2025bug7 (ADI/Siemens): Correction in BODYMOD definitions and related body current calculations.
- 2025bug8 (ADI): Removal of VAMPyRE errors/notices regarding model parameter definitions.
- 2025bug9 (ADI): Resetting values of variables after $error() statements.
- 2025bug10 (GF): Correcting NF dependency of flicker noise in FNOIMOD=1.
- 2025bug11 (UCB/IITK): Updating the QA tests for BODYMOD!=0 as per the fix of 2025bug7.
- 2026bug1 (UCB/IITK): Add checks on the binned parameters for negative values and updating model parameter macros for correct bound.
- 2026bug2 (Cadence): Remove redundant check on BODYMOD for warning statement regarding floating-body devices with fifth terminal as thermal node.
- 2026bug3 (GF): Add a warning for maximum device temperature.
- 2026bug4 (UCB/IITK): Update equation numbers and figures with better quality in technical manual.
- 2026bug5 (Synopsys): Correct the floating-body calculation for BODYMOD=0 and TNODEOUT=1 while the 5th terminal 'b' is a 'thermal' node.
- 2026bug6 (UCB/IITK): Update the QA tests to cover both body contacted and floating body cases.

L-UTSOI: 102.9.0

Developed by CEA-LETI

Bugs Fixes:

- BF1: NQS calculation: The second pole implementation has been updated to reduce large stamping values.
- BF2: Update the descriptions of the parameters and the unused macro.

Accuracy and predictability improvements:

- AP1: Introduction of gate resistance (introduction of RG for local model and RGO, RINT, RVPOLY, RSHG, DLSIL for global mode.
- AP2: Introduction of source, drain and well resistance (introduction of RSE, RDE and RWELL for local model and RSH, RSHD and RWELLO for global mode).

Changes in model inputs and outputs:

- IO1: MOS gate, source, drain and well resistance (intrinsic input resistance) OP-variables has been updated in accordance with introduction of gate resistance.
- IO2: Introduction of MULT_I, MULT_Q and MULT_FN.
- IO3: Introduction of NGCON, XGW, NRS and NRD.

Bipolar Transistor Models

MEXTRAM 505.6.0

Developed by Auburn University

Summary of Enhancements:

- A non-quasi-static (NQS) option EXMOD = 4 is added for the extrinsic base-collector diffusion charges Qex and XQex
- A floor 0.1 VT is added to the first denominator of Gmax (used when SWGEMLIM =1).
- Improvements in recovery of V^*_{B2C2} from $e^{V^*_{B2C2}/V_T}$
- Addition of the new parameter Vexlimr (default 400) and a two-sided macro `expLinlh` that linearizes exp() at both very positive (above Vexlim) and very negative (below -Vexlimr)

HICUM_L2 3.2.0

Developed by Dr. Michael Schroter

Enhancements:

- Defined NIST2018 physical constants in code
- RTOLC: `define RTOLC $simparam("reltol",1.0e-5)-
- GMIN: replaced `GMIN by real variable gmin
- Base current discontinuity in HICQFF:
    - eliminated conditional statement (if(itf>=1.0e-6*ick) ...)
    - re-arranged code in HICQFC to avoid division by zero
- Re-arranged implementations of saturation current T dependence re. improved computational efficiency
- Declaration of thermal node as thermal (instead of electrical) (& renamed (V,I) -> (Temp,Pwr))
- Set transfer current iteration tolerance RTOLC=reltol(sim.)-

- Added gmin to SC junction branch dep. on SOI/junction isol.

Gallium Nitride High Electron Mobility Transistor Models

MVSG_CMC 5.0.0

Developed by MIT, University of Waterloo

Updates:

- calc_ig modifications
    - Forward gate current calculation simplified while achieving nearly identical characteristics
    - Added branches for pg_paramin or fracin being zero
    - Fixed units for pg_paramd
    - Changed vgsat parameters to cz from oz
    - Added pg_paramin_inv to prevent divide by zero in some compilers
    - Temperature coefficients for forward mode inverse ideality factors
    - Temperature coefficients for reverse mode inverse ideality factors for gate leakage diodes
    - Clamp lower bound of inverse ideality factors in calc_ig to zero
    - Renamed alphag{} parameters for high injection smoothing to hinjs{} to avoid confusion with calc_iq alpha
- Redundant field plate parameter removal
    - Removed flagfp{s1,s2,s3,s4,1,2,3,4}s and cfp{s1,s2,s3,s4,1,2,3,4}s parameters as FPs on both source and drain sides can be utilized instead
    - Removed flagfp{s1,s2,s3,s4,1,2,3,4}b parameters so that ccfp{s1,s2,s3,s4,1,2,3,4} and cbfp{s1,s2,s3,s4,1,2,3,4} are turned off by setting to zero
    - Removed qsfp{s1,s2,s3,s4,1,2,3,4} local variables and contributions to I(gi2,si) which were for cfp{s1,s2,s3,s4,1,2,3,4}s capacitances
- Hardcoded legacy parameter flagsp to be not modifiable by the user
- M_MAXEXP value set to 37.0, used for ln(1+exp()) formulation as 1+exp(37) = exp(37) in double precision calculations
    - M_MAXEXP2 value using original value of 50.0 for other exp() calculations
- absfunc and mmax function changed to include flaggum parameter as input

- Revised charge trapping onset formulation to allow smoother transition. Added pgtrap and trapbeta
- Alpha fix
    - Allow weak to strong inversion parameter alpha{} to be set to zero to disable
    - Set default value of alpha{} parameters to be zero
- Separated rsh and rcs/rcd calculations and temperature coefficients
- Added wdeltas and wdeltad to allow deviations of SAR and DAR widths relative to intrinsic FET width
    - added check within code to ensure they are greater than -w, internal variables added
- Added temperature coefficient tcss for ss
- Revised DIBL equation to ensure monotonicity when delta2 engaged
    - New delta2 behaviour: fraction of delta1 that remains after dibsat
- Regrouped model parameters
- Parameter unit and description cleanup

ASM-HEMT 101.6.0

Developed by Macquire University

Summary of changes:

- Diode current computational stability improvement
- Cleaner code with several unused variables and equations streamlines
- Added global Gmin parameter to improve convergence
- Added new IDIO4 (new gatemod=4 formulation) for more accurate reverse-bias leakage
- Improved reverse-bias smoothing for better numerical stability

Bulk Planar CMOS Transistor Models

PSP 104.1.0

Developed by CEA-LETI

Summary of Changes:

- Implementation of a Vg dependence of the diode breakdown voltage and the diode BBT current for the gate-edge component. The related parameters are **ADVBRGAT**,

BDVRGAT, **ADBBTGAT** and **BDBBTGAT**. They are all declared in the not standalone branch of the JUNCAP200_parlist.include file. They exist in the drain side version by the addition of the letter D at their end.

- Implementation of the scaling factors MULT_I, MULT_Q and MULT_FN.
- Addition of parameters GC2OVD, GC2OVDO, GC3OVD and GC3OVDO and related equations to
- make the gate overlap current fully asymmetrical.
- Addition of parameters IMAXII and IMAXIIO to limit the impact ionization current.
- Bug-fix preventing NaN value for ysat
- Bug-fix preventing NaN value for nscr

BSIM4 4.8.3

Developed by UC Berkeley, IIT Kanpur

Enhancements:

- 2019enh3: CF is calculated based on the default value of TOXE, but not using updated value of TOXE (ADI, Infineon)
- 2021enh1: Description of U0 protection in BSIM4 manual (Primarius)
- 2021enh2: Checks on BSIM4phi, BSIM4phieot, and BSIM4tempeot (ADI)
- 2021enh3: Typo in intrinsic carrier concentration equation in the technical manual (ADI)
- 2022enh1: Typo in the BSIM4 technical manual for mobility model – MOBMOD = 3 (ADI)
- 2022enh2: ids0mult parameter (MULT_I, MULT_Q, MULT_FN) (GF/Cadence) 7. 2022bug1: Correction of if condition for BSIM4PhiBSWS parameter (ADI)
- 2022bug3: Missing new parameters (GIDLCLAMP / IDovVDSC) in b4mpar.c (UCB/NGSPICE)
- 2022bug4: Complete documentation of tempMod = 2 and 3 (ADI)
- 2023enh1: Inclusion of comprehensive QA test for MULT check (Cadence/BSIM group)
- 2023bug1: BSIM4 non-zero terminal current with all terminal voltage zero (NXP/Cadence)
- 2023bug2: Negative Cgg/Cbg at high Vdd, high back bias and negative keta (TI/Cadence)

- 2024enh1: Missing Details of Length/Width/Cross dependencies of binnable model parameters in BSIM4_4.8.3_beta1 Technical Manual (GF)

Bug Fixes:

- 2024bug1: Making bug-fix (2023bug2) backward compatible (ADI/Cadence)
- 2024bug2: Interpretation for default value of dW & dL parameters in BSIM4_4.8.3_beta1 Technical Manual (GF)
- 2024bug3: Missing lines in b4mask.c and b4ask.c to handle a few parameters (ADI).
- 2024bug4: BSIM4 version check (ADI).
- 2024bug5: Code update for developer's names (ADI).

Single and Multi-gate 3D Transistor Models

BSIM-CMG 112.1.0

Developed by UC Berkeley

Bugs Fixes:

- 2024bug10(Synopsys): Improved Vdsat Implementation to prevent floating point limitations
- 2025bug1 (Intel): Define separate length_scaling macro for CV parameters.
- 2025bug2 (ADI): Prevent divide-by-zero by QSREF_i
- 2025bug3 (Samsung): Update documentation to remove ETAQM.
- 2025bug4 (ADI): Multiple fixes for HVMOD=1
- 2025bug5 (ADI): Parameter limits depending on instance parameters
- 2025bug6 (ADI): Add error conditions for LeffCV/LeffCV_acc and Lg
- 2025bug7 (Synopsys): Correct TFIN dependence for Ies
- 2025bug8 (ADI): Make binned parameters `MPRnb with limit checks on the final binned variable
- 2026bug1 (Synopsys): Fix node assignment for RGATEMOD=2
- 2026bug2 (Intel): Multiple fixes for FNMOD=2

Enhancements

- 2024enh11(ADI): Using functions instead of macros for lln, lexp, and hypsmooth

- 2025enh1 (ADI, QA subcommittee): Extended QA to evaluate non-default parameter values.
- 2025enh2 (Intel): Improved gate resistance model
- 2025enh3 (GF): Improve capability to accurately model capacitance in FinFETs/GAAFETs with LDD
- 2025enh4 (Intel, ADI): Improvements in documentation
- 2025enh5 (Intel): Adjust limits to muhc0 and muhc1
- 2025enh6 (ADI): Update QA suite to prevent noise output clipping below threshold levels.
- 2025enh7 (Intel): Improve the flicker noise model to offer flexible dependence on mobility/QM parameters

Resistors, Diodes, Varactor

MOSVAR: 1.4.0

Developed by Arizona State University, Sentinel IC Technologies, TowerJazz Semiconductor, Freescale Semiconductor

Summary of Changes:

- Changed IGMAX warning to check only dc current.
- Added SWQINV to enable switching off Qinv calculation.
- Added aliases DTEMP (for DTA) and TREF (for TR).
- Updated macros ‘MINA and ‘MAXA.

Diode_CMC: 3.0

Developed by Hiroshima University

Summary of Changes:

- Scaling of internal nodes
    - Added scaling for internal NQS nodes charge_a, charge_k, and depl_a.
    - Scaled node potentials and flows to align with typical voltage and current magnitudes used by simulators.
    - Improved compatibility with simulator absolute tolerances, enhancing simulation robustness and convergence.

    - No impact on the diode model’s electrical characteristics.
    - Scaling factors can be customized by EDA vendors to optimize simulator performance.
- Parameter Limits
    - The upper limit of the model parameter 'inj2' has been increased from 20 to 50, allowing for a wider range of values to be used.
    - The minimum value for the parameter 'tau' has been set to 1.0e-12 to avoid division by zero errors.
    - The value of the macro 'vbrmax' has been changed from 1000 to 1.0e+06.
- New parameters/macros
    - A new model parameter 'swbv' has been introduced to enable breakdown, along with an alias parameter 'bv_enable'.
    - A new emission coefficient parameter 'nj0' has been introduced (nj at VAK=0V), which allows the diode current Id to be exactly 0A for Vd=0V.
    - The macro ‘c_esi’ has been replaced by internal variable ‘EPSSI’ for consistency.
    - The macro 'MINRES' has been replaced by the model parameter 'minr', which can be set by the simulator. If not set, 'minr' defaults to 0.
- Removed parameters
    - The model parameter 'type' has been removed, as changing p/n-type can be done by changing polarity.
    - The parameter 'mult' has been removed, as the multiplier 'm' can perform the same function.
- Other Changes
    - In the equation 'Vjunc_A = PB - VAK', PB (fixed to 0.6) has been replaced by ‘vbirbot_i’ for consistency
    - The information in the MP macros for 'inj1' and 'inj2' has been updated to provide more accurate descriptions. inj1: "Factor for recovery charge density" inj2: "Voltage dependence of recovery charge density (high injection)"
    - Measures have been implemented to ensure that 'minr=0' is possible for all combinations of series resistance parameters.
    - The condition for serial resistance calculation has been changed to ‘(restotal > 0 && restotal >= minr)’.
    - 5.5 Lowercase letters have been introduced for all model and instance parameters and node names to comply with the CMC Verilog-A code standard policy.

ESD Diode Model

ASM-ESD: 101.1.0

Developed by Macquire University

Summary of Release Notes:

- Code structure changes
    - Two separate *.va files asmesd.va and asmesd_dio.va created as opposed to one *.va files in last release.
    - Two include files asmesd_parameter.include and asmesd_macros.include added in this release.
- Update to Tfail parameter upper limit
- Vbesat and veesat formulation update for Rb and Re
- Use Bf_t in transit time calculations
- Use abs() in Dkqb with pow() function
- Minr model parameter with protection for divide-by-zero added
- Qdeformulation update
- Tff formulation update
- Minr and resistance condition update for VAMPyre warning
- Texp parameter definition update to avoid divide-by-zero
- Asmesdm_parameters.include change
- Asmesd.va changes
- Asmesd_dio.va changes
- Asmesd_parameters.va changes