

THE SILICON INTEGRATION INITIATIVE 2025-2026 REPORT

A Not-for-Profit Membership Organization

Suppliers and users who innovate on trusted standards
and share solutions that lower development costs and
increase design productivity

Si2



SI2 PURPOSE

“Provide collaborative technology and services which enable higher levels of semiconductor design integration leading to industry-accepted standards. It is the intent of this initiative to make any such standards, technology, and services available to all who are interested at a fair and reasonable cost.”

VALUE

- Influence
- Lower Costs
- Design Efficiency
- Differentiation



A MESSAGE FROM OUR CEO

Si2 is a not-for-profit membership organization created for the benefit of our members. We are a community of over 70 EDA tool suppliers & users from industry and 12 academic members who innovate on trusted standards and share solutions that lower development costs and increase design productivity. With our members, we provide collaborative technology and services which enable higher levels of semiconductor design integration leading to industry-accepted standards. We make such standards, technology, and services available to all who are interested at a fair and reasonable cost. Our members enjoy **greater influence** by interacting with other industry leaders, **lower development costs** by leveraging Si2 resources, **greater efficiency** via unlimited use of Si2 solutions in their companies, and **greater differentiation** via access to source code and redistribution rights for Si2 solutions when implemented as a component of the member's production-level software application.

In the last year, we saw great results and growth. The **OpenAccess Coalition** (OAC) now supports 55 member companies and will soon enable greater participation from academia. The **Compact Model Coalition** (CMC) hosted the second International **Compact Modeling Conference** (ICMC) while delivering 7 production model releases. The scope and membership in the **Unified Power and Thermal Coalition** (UPTC) grew. We published the inaugural LBC-Leaderboards in support of **the LLM Benchmarking Coalition** (LBC) that will expedite development of high-quality LLMs for semiconductor design. Our **AI/ML SIG** initiated a seminar series and continued to investigate overcoming bottlenecks in applying AI in SoC design flows. Our **AI/ML Schema Openstandards working group** released the first implementation of a vendor-neutral ontology on GitHub that will enable vendor-agnostic algorithms & app development. Finally, our **3DIC** efforts continue to focus on providing key inputs to the IEEE P3537 3Dblox work group.

There is a lot going and I hope the following pages provide a little more detail. I want to thank our members for their continued participation and leadership. This not only provides value to them but also allows the semiconductor industry to grow.

Robert Aslett
CEO, President



A MESSAGE FROM OUR VP OF TECHNOLOGY

2026 was a year with a sense of urgency – **Si2 releases of standards and reference implementations** are more important than ever as AI and Agentic Flows change the semiconductor ecosystem.

The focus of the **Si2 LLM Benchmarking Coalition** with leaders Nate Pinckney, Nvidia, and Ramesh Narayanaswamy, Synopsys, has moved with industry from LLM benchmarking to include Agentic Flows. Our December 2025 workshop confirmed the LBC Working groups: **Extending and Expanding** the CVDP benchmark, defining critical next steps for **interoperability**, and developing a production Leaderboard for CVDP and extensions. At DAC 2026, over 70 people attended the LBC Forum to hear the **announcement of the LBC-bench Leaderboard** and an industry panel on **“Aligning Agentic Benchmarking and Verification Methods with Real-World EDA Workflows.”** This was also our July 2026 2nd LBC workshop theme, with keynotes, invited speakers, and panelists featuring **calls to action on end-to-end chip design benchmarking and metrics for agentic flows**. Join us as we work with our growing team of industry and academic members to realize these goals!

The **Si2 Unified Power and Thermal Coalition** sponsored a DAC 2026 hands-on tutorial given by Ali Sadigh and Dominic DeMarco, Si2, and Prof. Rhett Davis, NC State, where **attendees ran the newly published IEEE 2416-2025 “IEEE Standard for Power Modeling to Enable System-Level Analysis” reference implementation power calculator from Si2**, illustrating the advantages of this power modeling format for system-level analysis. See [Si2 on YouTube](#). Be sure to try the release of the reference implementation, UPM PowerCalc, later this year!

The **International Compact Modeling Conference 2026** took to the seas on the Queen Mary in Long Beach, CA for the 2nd successful year, led by Shahed Reza, Sandia and Gert-Jan Smit, NXP. Over 80 attendees participated in the conference **uniquely focused on semiconductor device modeling** with a range of deep, technical topics including a panel on AI in Compact Modeling. Look for the Call for Papers: ICMC 2027, July 15-16 in San Jose, CA.

Dr. Leigh Anne Clevenger
VP Technology





A MESSAGE FROM OUR SR DIRECTOR OF OA

AI figured it out! After 23 years of communicating the value of **OpenAccess** in the EDA space AI provides a another means for potential members to understand the complex value of the OpenAccess Coalition. OpenAccess, by nature, contains deep technical concepts (**interoperability, extensibility, rapid prototyping, ease of integration, etc.**) which make it hard to communicate the value to potential members who only need to know the part that pertains to them. I always say, “Tell me who you are, and I can tell you what you need to know about OA, otherwise we will be here all day”. AI tailors public information to the user’s need with its Socratic interrogation style. It filters 23 years of public content in cyberspace and tells the potential member only what pertains to their situation. Our calendars are now full with potential member discussions and onboarding meetings, which is a good problem to have. Ten new member companies are developing **AI based EDA applications** and more inquire about membership every day.

DAC 2026 OA Forum had five AI based member presentations (See [Si2 on YouTube](#)) and some could not make the time frame for presentations. One presentation was completely generated by AI tools with minimal input from the member. Another presentation was in perfect English by a non-English speaking engineer and I challenge you to figure out which of them it was.

OpenAccess Coalition Workshop 2026 focused on difficult OpenAccess topics (**Pcells, Constraints, Techfiles use, Wrapping C++**). All presentations this year were done by Si2 Engineerrrs. This is the team that helps you when you find an issue in OpenAccess Reference Implementation or one of the extensions to the API. The Si2 Engineering resources will be supported next year by **new Si2 IT Infrastructure**.

Cautious AI adoption is our mantra moving forward. OA is proprietary and can not be made public through LLM training. Protecting information is an industry-wide problem and we must retain a leading-edge position to protect our member’s investment. This requires legal advice, member education, as well as finding and implementing best practices.

Marshall Tiner
Sr. Director of OpenAccess



SI2 2025-2026 HIGHLIGHTS

- [LLM Benchmarking Coalition](#): Announced [LBC-bench Leaderboards](#) with CVDP benchmark results
- [Compact Model Coalition](#): 9 production model releases; 2nd annual [International Compact Modeling Conf](#)
- [OpenAccess](#): 4 OA Ref Implementation & 3 OA Extension releases; AI-centric DAC26 Forum, '26 Workshop
- [Unified Power Model](#): Co-developed a dynamic power methodology and re-architected UPMPowerCalc
- Released the initial [AIML Schema Ontology](#) for public evaluation and refinement
- Initiated a technical speaker series for Si2 members focused on Agentic AI for production design
- Co-led deep dive team on IEEE P3537 3Dblox standard specification additions
- Si2 membership grew to over 72 corporate and 12 academic members with more in process

THE SI2 BOARD OF DIRECTORS 2026-2027

1	Leon Stok (Chair)	IBM
2	Lu Dai (Treasurer)	Qualcomm
3	Jacob Avidan	Synopsys
4	Niels Fache	Keysight
5	Wilbur Luo	Cadence
6	Mo Movahed	Siemens
7	Viraphol Chaiyakul	NXP

8	Manoj Selva	Intel
9	Thomas Ahle	Normal Computing
10	Aveek Sarkar	TSMC
11	Gaurav Varshney	Texas Instruments
12	J.Y. Choi	Samsung
13	Bang-hyun Sung	SK Hynix
14	Jim Culp	Global Foundries
15	Rob Aslett	Si2 CEO, President

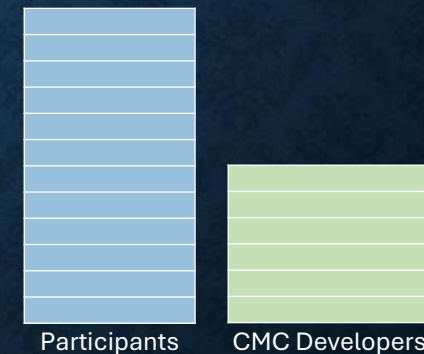
72 CORPORATE & 18 ACADEMIC MEMBERS

When industry collaboration is needed, the Si2 community provides the means to deliver more value to its members than they can achieve alone



Corporate Member Profile

Note: some companies show up in more than one column



Academic Member Profile

MEMBER DRIVEN GOVERNANCE

Si2 Board of Directors

Chair: Leon Stok Treasurer: Lu Dai Viraphol Chaiyakul	IBM Qualcomm NXP	Wilbur Lou James Culp Manoj Selva Niels Faché	Cadence GF Intel Keysight	Thomas Ahle Jung Yun Choi Mo Movahed Banghyun Sung	Normal Computing Samsung Siemens SK Hynix	Jacob Avidan Aveek Sarkar Gaurav Varshney	Synopsys TSMC TI
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Tech Steering Group	
Chair: Kerim Kalafala	IBM
Solaiman Rahim	Synopsys
Vivek Rajan	Intel
Aparna Dey	Cadence
Narasimhan Narayan	NXP
Chris Mueth	Keysight

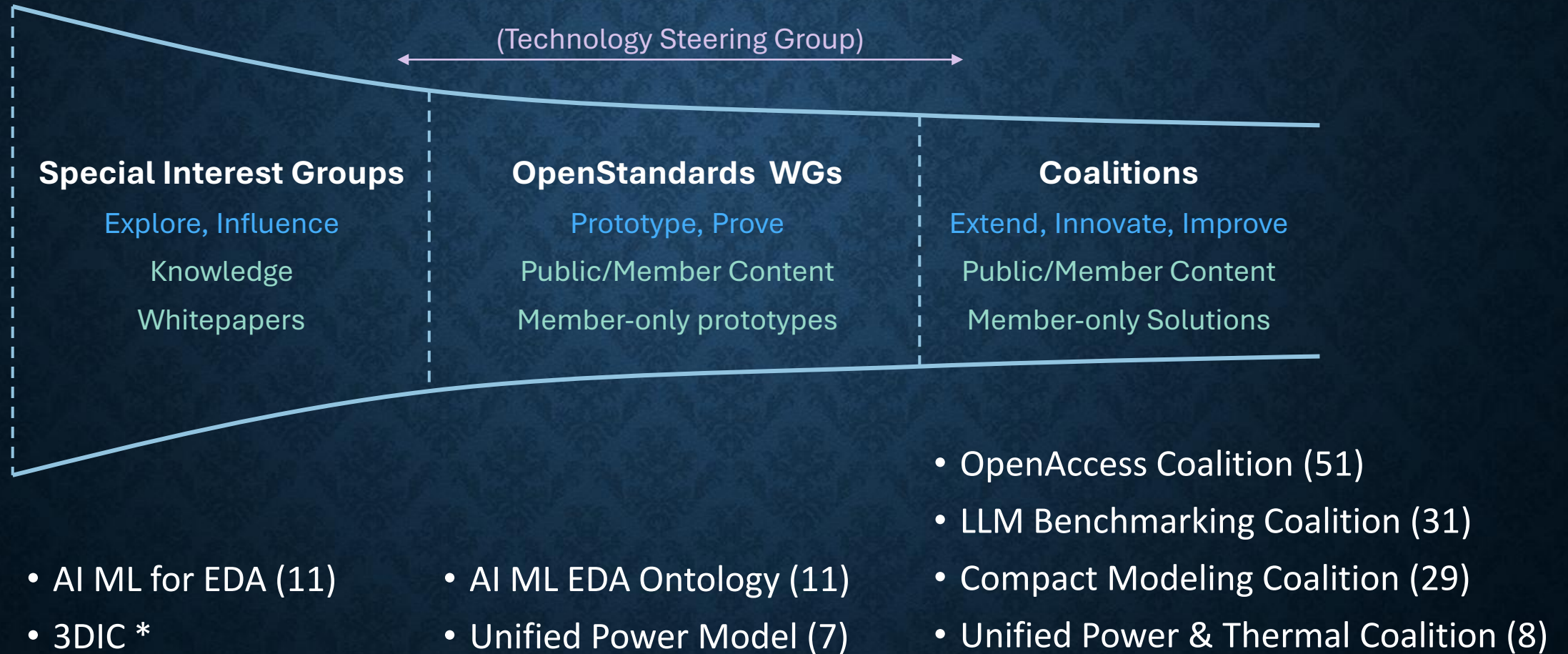
WGs & SIGs	
UPM WG	
Chair: Nagu Dhanwada	Google
AIML EDA Ontology WG	
Chair: Ivan Kissiov	Siemens
AIML for EDA SIG	
Chair: Akilesh Kumar	Synopsys

Coalitions	
OpenAccess	
BOD Chair: Shiwain Kaul	Intel
BOD Vice Chair Sriram Sivasubramaniyan	NVIDIA
BOD Rep: Haijun Fang	TSMC
BOD Rep: Diego Garcia	Keysight
BOD Rep: Yong Hwan Jeon	SK Hynix
BOD Rep: Zhiying Chen	IBM
CT Co-Arch: Mark Rossman	Cadence
CT Co-Arch: Adam Matheny	IBM
ESG Chair: James Masters	Intel
Unified Power & Thermal	
Chair: Nagu Dhanwada	Google
Acting	
Compact Modeling	
Chair: Peter Lee	Micron
Vice Chair: Jushan Xie	Cadence
Treasurer: Takeshi Naito	Kioxia
Secretary: Tanvir Morshed	Rapidus
Model QA: Shahriar Moinian	Broadcom
Advisor: Geoffrey Coram	Analog Devices
LLM Benchmarking	
Chair: Nate Pinckney	NVIDIA
Vice Chair: Ramesh Narayanaswamy	Synopsys
Leader Board WG: Chinmay Hegde	NYU
Extend/Expand WG: Nate Pinckney	NVIDIA
Interoperability WG: Ehsan Degan	IBM

42 Leaders from
20 Companies &
Universities



SI2 PROGRAM MATURITY



* 3D IC SIG engagement is via the IEEE 3537 WG

SIG & WG HIGHLIGHTS

SIGs

3DIC

Explore opportunities for standards and shared utilities

Si2 co-led deep dive team on IEEE P3537 3Dblox standard specification additions

AI/ML for EDA

Explore the best way to apply AI and ML for chip design

Initiated a technical speaker series focused on Agentic AI for production design (Ontology, EDA-specific hallucinations etc..)

OS WGs

UPM

Propose refinements to the IEEE 2416 standard for complex designs

Delivered tutorial of the IEEE 2416-2025 System reference implementation of the UPM PowerCalc utility at DAC 26

AI/ML EDA Ontology

Provide a semantic foundation for AI-driven EDA

Made a public release of EDA Ontology developed by the WG that provides the reasoning backbone for agentic systems for EDA

COALITION HIGHLIGHTS

CMC

Compact Model
Coalition

Selection & continuous
improvement of industry
standard compact SPICE
models

Delivered 7 production model releases and 29 Beta releases in
last 12 months

UPTC

Unified Power &
Thermal Coalition

Proliferation of system
level power utilities and
methods in support of IEEE
2416 UPM

Developed a Dynamic Power methodology with Samsung
Foundry and made UPM PowerCalc available

OAC

OpenAccess Coalition

Continuous improvement
of the world's most widely
used open reference
design database

Developed "AskOA" for academia; AI-centric EDA Forum
presentations at DAC26 Forum; Workshops on difficult
concepts; Made 4 OA and 3 Extension releases; fixed 6 issues.

LBC

LLM Benchmarking
Coalition

Benchmarks & metrics for
verification of agentic
flows and systems for
semiconductor design

LBC-bench Leaderboard announced with CVDP benchmark
results; Added four contributors (so far) to help extend and
expand the content

2026 POWER OF PARTNERSHIPS AWARD



Si2's annual Power of Partnership (POP) award is a testament to the power of collaboration in our industry.

It spotlights the essential role that volunteer teams play in Si2's continued success.

It is presented annually to a volunteer team that has made the most significant contribution to the success of the electronic design automation industry.



2026 POWER OF PARTNERSHIPS AWARD

NATE PINCKNEY (NVIDIA)

RAMESH NARAYANASWAMY (SYNOPSYS)

EHSAN DEGAN (IBM)

CHINMAY HEGDE (NYU)

FOR LAUNCHING THE LLM BENCHMARKING COALITION
(LBC) AND OVERSEEING ITS EXPANSION AND
EXECUTION

PINNACLE AWARD WINNERS

The quarterly Si2 Pinnacle Award recognizes volunteers for their significant professional contributions to Si2 programs

Q3 2025: Jeff Brubaker (Synopsys): For his instrumental insights and contributions in the OpenAccess Coalition Change Team

Q4 2025: Rajiv Subramanian (Intel): For contributions to several OpenAccess extensions, such as track patterns, the polygon operators, coloring, as well as others .

Q1 2026: Prof. Vidya Chhabria (Arizona State Univ) and Prof. Ioannis Savidis (Drexel Univ): For their significant contributions to the Si2 AI/ML Schema OpenStandards Working Group

Q2 2026: Mark Rossman (Cadence): For moving the OA change team forward through three data model versions and many more minor releases while enabling improved cross correlation of member issues.

OUTSTANDING CONTRIBUTION AWARDS

The Si2 Outstanding Contribution Award recognizes continuous contribution to Si2 and the semiconductor industry over many years

Jerry Frenkil Honored with Si2 Outstanding Contributions Award: For his technical and executive leadership for 40 years in semiconductor EDA low-power analysis

Terry Berke Honored with Si2 Outstanding Contributions Award: For his dedication and success in semiconductor marketing and communications for over 25 years

Ramond (Ray) Rodriguez: For chairing the OpenAccess Coalition Board where he made significant contributions to the semiconductor industry and was a role model for collaboration

SI2 SESSIONS AT DAC 26



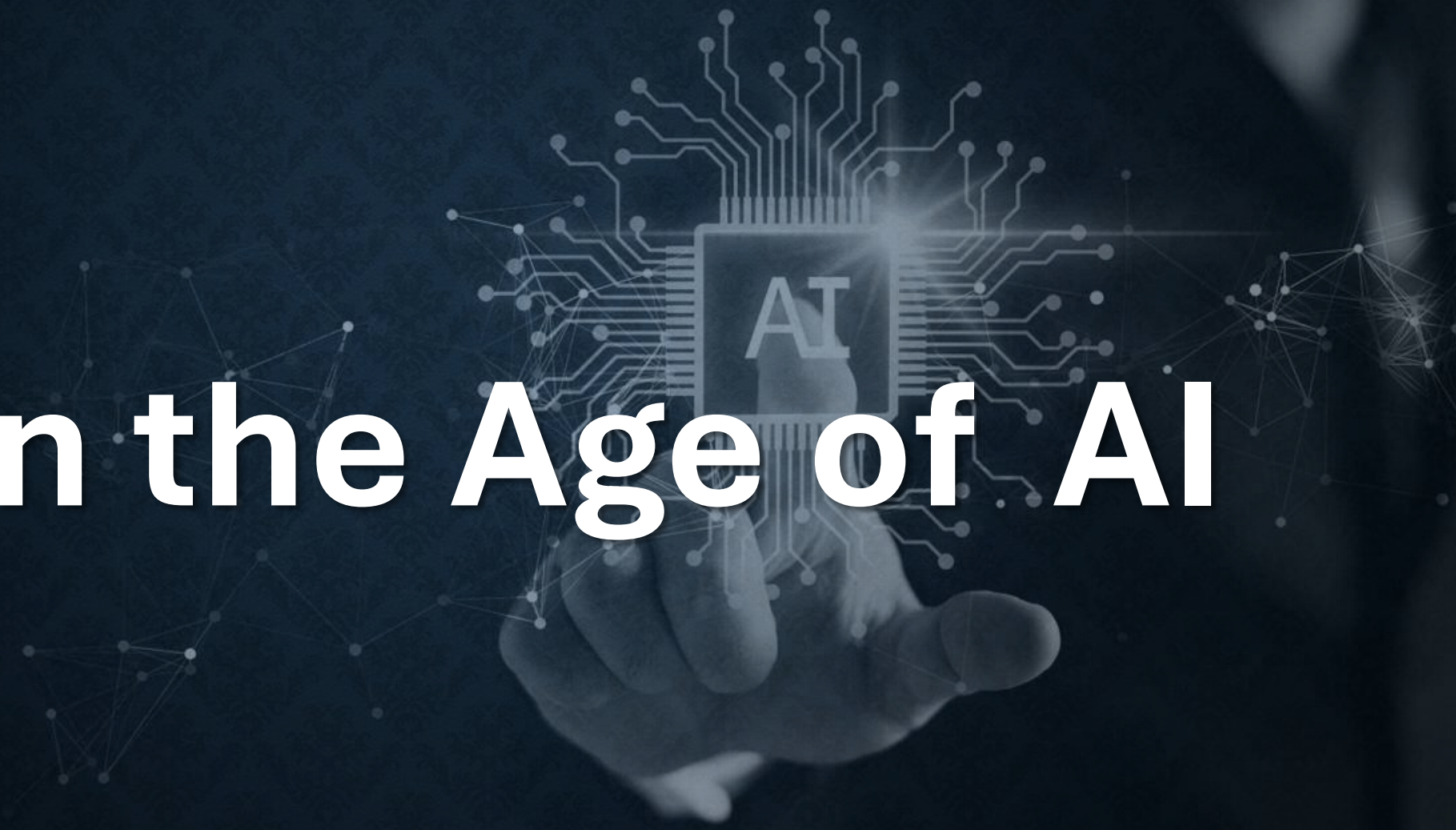
SI2 SPONSORED INTERNATIONAL COMPACT MODELING CONFERENCE



LBC WORKSHOP



Si2 in the Age of AI

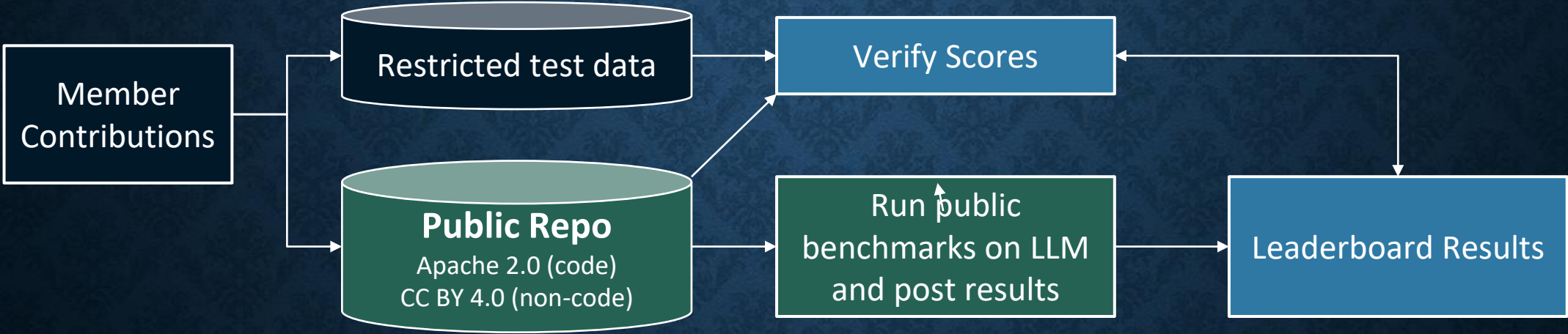
A conceptual image featuring a hand pointing towards a glowing square chip with the letters 'AI' on it. The chip is surrounded by intricate circuitry and a network of nodes connected by lines, all set against a dark blue background.



The LLM Benchmarking Coalition

Purpose

Expedite the development of high-quality LLMs for semiconductor design by creating relevant and comprehensive evaluation datasets and metrics for semiconductor design problems.



Si2 Staff

Members

Public



Leaderboard <https://lbc-bench.si2.org/>

CVDP Dataset

LBC-bench

Leaderboards

BENCHMARKS

Code Generation

Code Comprehension

Context Heavy

ABOUT

Paper

CVDP Benchmarks GitHub

CVDP Benchmarks Hugging Face

Press

Si Leaderboards

Code Generation Limited ContextCode ComprehensionCode Generation Heavy Context

Filters: All TagsAll ReleasesSearch...

Model	% Resolved Full	% Resolved OSS	Org	Avg. \$	Date	Notes	Logs/Trajs	Site	Release
Gemini 3.1 Pro Preview	81.31	81.31		-	2026-05-10		-		1.1.0
gpt-5.2 high reasoning	75.46	75.46		0.56	2026-02-19				1.0.2
o4-mini	74.91	74.91		0.13	2025-11-10				1.0.2
Gemini 3.1 Flash Lite Preview	74.75	74.75		-	2026-05-10		-		1.1.0
gpt-5.2 medium reasoning	74.57	74.57		0.33	2026-02-09				1.0.2
gpt-5.2 low reasoning	74.37	74.37		0.19	2026-02-10				1.0.2
Gemini 3.1 Pro Preview	73.47	73.47		-	2026-04-08		-		1.0.2
Kimi K2.5	72.03	72.03		-	2026-04-08		-		1.0.2
gpt-5-mini	72.00	72.00		0.04	2026-01-23				1.0.2
claude-sonnet-4-5-20250514	70.83	70.83		0.21	2025-12-08				1.0.2
Gemini 2.5 Pro	69.11	69.11		-	2026-04-08		-		1.0.2
gpt-4o-mini	68.55	68.55		0.03	2025-11-10				1.0.2
claude-sonnet-4-5-20250929	67.22	67.22		0.26	2025-12-06				1.0.2
GPT-5.3 Codex	67.04	67.04		-	2026-04-08		-		1.0.2
Claude Opus 4.6	64.23	64.23		-	2026-04-08		-		1.0.2
Claude Sonnet 4.6	64.00	64.00		-	2026-04-08		-		1.0.2

CVDP Infrastructure
Website codebase

Platform

si2org/lbc-be

CodeIssues

main2

si2admin Merge

.github/workflow

css

data

img

js

scripts

templates

.gitignore

CNAME

LICENSE

Makefile

README.md

README_CONTRI

build.py

favicon.ico

pyproject.toml

uv.lock

npft Update

docker

example_da

examples

src

tests

tools

.env.example

.gitignore

CONTRIBUT

LICENSE

LOCAL_INFERENCE_GUIDE.md

NOTICE

README.md

README_AGENTIC.md

README_DEVELOPER.md

initial-commit-v110 months ago

Hugging Face

Search models, datasets, ModelsDatasetsSpaces

Datasets: nvidia/cvdp-benchmark-datasetlike32Follow

Modalities: TextFormats: jsonSize: <1KLibraries: Datasetspandas

Dataset cardData StudioFilesxetCommunity

Dataset Viewer

Subset (6)cvdp_agentic_code_generation_c...68 rowsSplit (1)eval68 rows

Search this dataset

id	categories	system_message
cvdp_agentic_64b66b_codec_0007	["cid013", "medium"]	You are a lang model that has
cvdp_agentic_8b10b_codec_0001	["cid003", "hard"]	You are a lang model that has
cvdp_agentic_AES_encryption_decryption_0020	["cid014", "medium"]	You are a lang model that has
cvdp_agentic_Min_Hamming_Distance_Finder_0003	["cid005", "hard"]	You are a language model
cvdp_agentic_Min_Hamming_Distance_Finder_0007	["cid013", "medium"]	You are a language model
cvdp_agentic_alu_0003	["cid014", "hard"]	You are a language model

typo in LOCAL_INFERENCE_GUIDE.mdlast year

Adding in example datapoints with ...last year

Updating README.md for heavy co...last month

Simplify explicit agent auth passthru...2 months ago

Moving additional documentation t...last year



The AI/ML EDA Ontology

Purpose

Provide a semantic foundation for AI-driven EDA, addressing the fundamental challenge that schema-based representations fail to capture: machines need semantic understanding, not just structural access.

THE EDA ONTOLOGY PUBLIC RELEASE

An OWL/Turtle ontology that allows EDA entities, flow stages, constraints, metrics, and meta data to be represented in a machine-readable and logically structured form that computers can understand and reason about.

Includes three use cases:

MCP – demonstrate how an MCP server/client can expose ontology semantics to agents, SPARQL queries, and LLM tools.

ASU – show how Croissant + ontology mappings generate timing datasets from CircuitOps CSVs and feed ML models.

Drexel – mirror the Drexel EDA-ML graphs to illustrate graph learning with ontology-backed semantics.

https://github.com/si2org/AIML_Schema_Ontology

The screenshot shows the GitHub repository page for `si2org/AIML_Schema_Ontology`. The repository is public and has 8 stars, 1 watching, and 0 forks. The main branch is `main` with 1 branch and 0 tags. The repository contains a file tree with the following files and their last commit dates (all 3 months ago):

File	Last Commit
<code>ontology</code>	Initial check-in of AIML schema ontology
<code>usecases</code>	Initial check-in of AIML schema ontology
<code>.gitignore</code>	Initial check-in of AIML schema ontology
<code>.gitlab-ci.yml</code>	Initial check-in of AIML schema ontology
<code>LICENSE</code>	Initial check-in of AIML schema ontology
<code>README.md</code>	Initial check-in of AIML schema ontology

The `README` file is selected, showing the title "Si2 AI/ML Schema Ontology Repository" and the following text:

This repo captures the Si2 AI/ML schema working group's release: a monolithic EDA ontology plus three first-class use cases (MCP, ASU, Drexel) that demonstrate how to apply it. Each directory is self-contained with adjacently located documentation and tests so you can stand up the ontology and its use cases without hunting for collateral elsewhere.

- `ontology/` publishes the canonical OWL/Turtle definitions and ontology-level tests.
- `usecases/MCP/` shows how to expose the ontology via a Model Context Protocol (MCP) server for agentic flows.
- `usecases/ASU/ASU_ML_EDA_data_flow/` implements the CircuitOps-inspired Croissant + ontology data pipeline used for timing ML.
- `usecases/Drexel/` mirrors the Drexel EDA-ML tasks for graph-learning.

The right sidebar shows the repository's metadata:

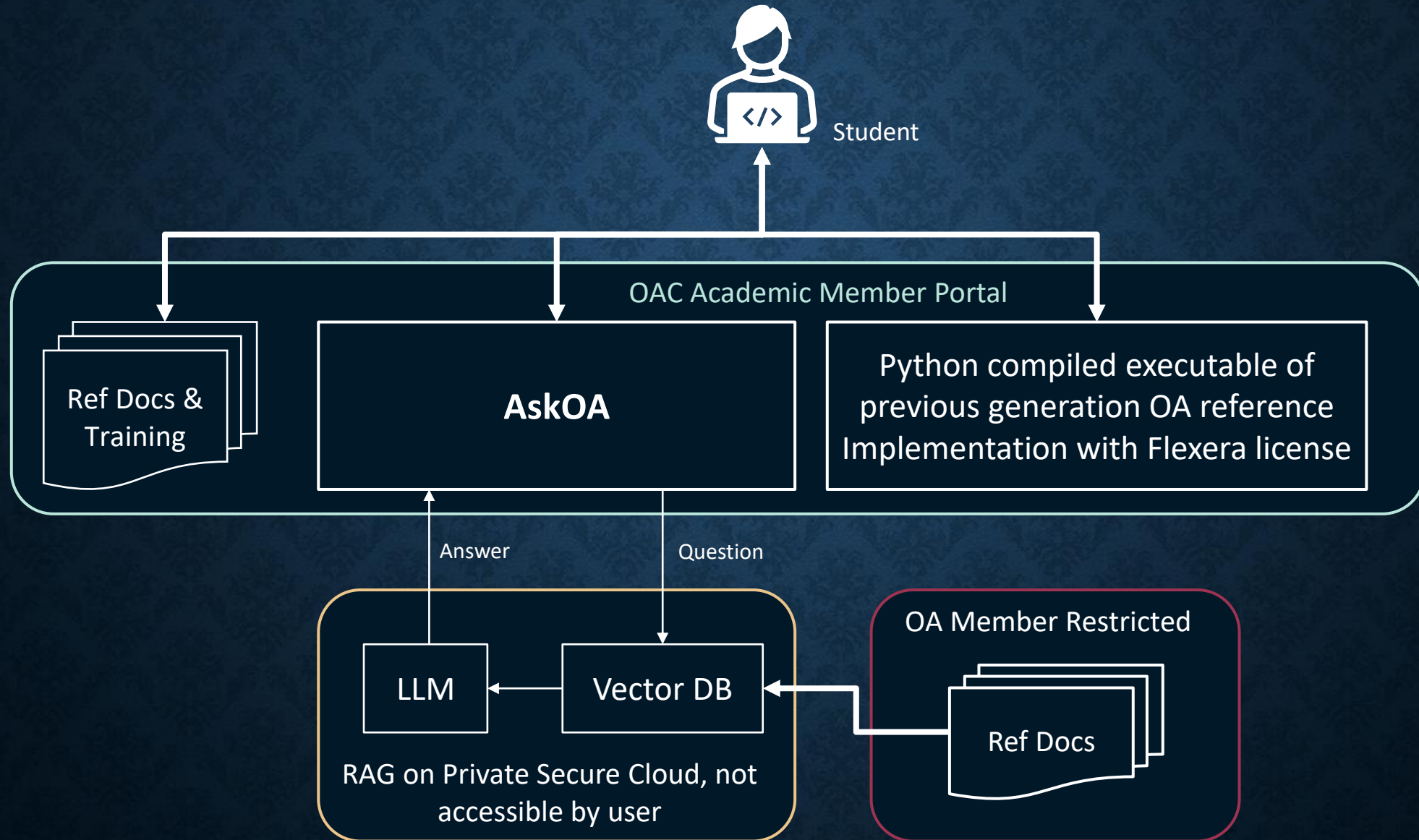
- About:** AIML Schema Ontology, Readme, Apache-2.0 license, Activity, Custom properties, 8 stars, 1 watching, 0 forks, Report repository.
- Releases:** No releases published.
- Packages:** No packages published.
- Contributors:** No contributors.
- Languages:** Python 58.3%, Verilog 37.4%, Shell 2.4%, Tcl 1.1%, Makefile 0.8%.



“AskOA” for Academia +

Purpose

Provide a secure and easy means for University students to
access and experiment with OpenAccess



The AI/ML for EDA SIG

Purpose

Share non-confidential knowledge, explore trends & topics of mutual interest,
and make recommendations for industry collaboration and standards

RECENT AIML EDA SIG DISCUSSIONS

EDA foundation model

Vocabulary Hallucination Issues

Role of Ontology

Long-Running Agentic AI Tasks and Metrics

General/Foundation LLM Limitations

Deployment Realities and Multi-Vendor Ecosystems

Maturity Ladder and Autonomous Task Guidance

Knowledge base curation for grounding LLMs

AI-Friendly Documentation and Best Practices

Agent Skills for EDA - General purpose Skills which should be available for any EDA flows.



Si2

A Not-for-Profit Membership Organization

Suppliers and users who innovate on trusted standards and share solutions that lower development costs and increase design productivity