

# THE SILICON INTEGRATION INITIATIVE 2024-2025 REPORT

<u>Si2</u>





# A MESSAGE FROM OUR CEO

Si2 is a not-for-profit membership organization created for the benefit of our members. We are a community of over 65 EDA tool suppliers & users from industry and academia who innovate on trusted standards and share solutions that lower development costs and increase design productivity. With our members, we provide collaborative technology and services which enable higher levels of semiconductor design integration leading to industry-accepted standards. We make such standards, technology, and services available to all who are interested at a fair and reasonable cost. Our members enjoy **greater influence** by interacting with other industry leaders, **lower development costs** by leveraging Si2 resources, **greater efficiency** via unlimited use of Si2 solutions in their companies, and **greater differentiation** via access to source code and redistribution rights for Si2 solutions when implemented as a component of the member's production-level software application.

In the last year, we saw great results and growth. The **OpenAccess Coalition** (OAC) now supports 51 member companies with 237 participants. The **Compact Model Coalition** (CMC) hosted the first International **Compact Modeling Conference** (ICMC) while delivering 10 production model releases. The scope and membership in the **Unified Power and Thermal Coalition** (UPTC) grew. We formed **the new LLM Benchmarking Coalition** (LBC) that will expedite development of high-quality LLMs for semiconductor design. Our **AI/ML SIG** is exploring topics such as bottlenecks in applying AI in SoC design flows and our **AI/ML Schema Openstandards working group** is close to providing a vendor-neutral ontology that will enable vendor-agnostic algorithms & app development. Finally, our **3DIC** efforts are now focused on providing key inputs to the IEEE P3537 3Dblox work group.

There is a lot going and I hope the following pages provide a little more detail. I want to thank our members for their continued participation and leadership. This not only provides value to them but also allows the semiconductor industry to grow.

Robert Aslett CEO, President





# A MESSAGE FROM OUR VP OF TECHNOLOGY

This year showed the result of great vision in the Si2 member leadership with quick response to industry needs for LLM benchmarking, Si2 hosted events at DAC, and the inaugural ICMC conference.

The new Si2 LLM Benchmarking Coalition is on track to positively impact research and development in semiconductor design. Using the new NVIDIA CVDP benchmarks as an open-source base, the coalition will expand to new problem sets and design domains. A dedicated leaderboard for benchmarks will provide metrics on LLM quality, with coalition members providing inputs from a wide range of companies and universities. I encourage your company to join in the conversation – have your voice and interests represented in this crucial, fast-moving area!

Nagu Dhanwada, IBM, chair of the UPTC made vision reality in a DAC Tutorial - the culmination of the UPM Proof-of-Concept projects with Qualcomm and Samsung Foundry and realization of a **full AMS system-level demonstration**. Daniel Cross, Cadence, Rhett Davis, NC State, and Ali Sadigh, Si2, combined created a new single-pass power analysis methodology. DAC Tuesday Si2 hosted other presentations including a well-received **industry/academic Lunch Panel**, "Powering the Future of AI: Are Standards an Enabler or a Bottleneck?"

The **ICMC** has been over 2 years in discussion, and the vision of general chair Peter Lee, Micron, and TPC chair Colin Shaw, Silvaco, paid off, with 80 attendees and a great satisfaction rating! I talked to many attendees who said this was a unique conference, with the **focus on compact model research and applications** – at other conferences this is only a side topic. The commitment and collaboration in the organizing committee provided attendees a quality experience, and we are already planning for **ICMC 2026**.

Dr. Leigh Anne Clevenger VP Technology





# A MESSAGE FROM OUR SR DIRECTOR OF OA

The OpenAccess Coalition may indeed have the most **unique business model**. The business model has revenue-based costing to foster startup innovation while still **sustaining viability** through a collaborative change process. The change process has reduced product variation ("forking") of the API. Minimization of this variation drives the **interoperability** between different member's applications.

In this, our twenty second year, the OpenAccess API is still viable for new design tool development. Due to the interoperable position in the EDA marketplace and it will soon become **the best way to feed the coming AI models** that will be utilized by our design tools.

Being the common database, Al models can source data from a single database and retrieve results from multiple tools in one place. To that end, we have the right features ready to enable these new technologies. The OpenAccess Coalition is poised to become the primary enabler for Al in EDA.

In support of the coming AI EDA tool needs we have driven the platform matrix forward to C++ 20 and Red Hat Eight level platforms as our baseline. Our Data Model Six partitioning feature becomes central to parallel processing enabling data collection with small execution cost. The OpenAccess fast query features lend themselves to hierarchy independent searches and quick data comparison.

To summarize the past year, we have **positioned the OpenAccess Coalition for the coming growth** of the EDA industry and accommodate the coming new technologies.

Marshall Tiner
Sr. Director of OpenAccess

# **SI2 2024-2025 HIGHLIGHTS**

- Formed the <u>LLM Benchmarking Coalition</u> to improve LLMs for semiconductor design
- Held inaugural International Compact Modeling Conference in San Francisco, CA
- Updated CMC Models: ASM-ESD, BSIM-BULK/4/CMG/IMG/SOI, HiSIM HV, MEXTRAM, PSP & OMI
- Updated the <u>OpenAccess</u> platform matrix to C++20 & RHEL 8 to support the Al and cloud era
- Released / testing new OA extensions: oaxColor, oaScript, polygon operators, oa2json & json2oa
- Delivered system-level <u>Unified Power Model</u> demo at DAC for a complex mixed-signal system
- Defined ontology & illustrated a tool flow that connects EDA and ML in the AI/ML Schema WG
- Shared EDA foundational model knowledge and set ICLAD 2025 panel topics in the AI/ML SIG
- Contributed improvements and helped expand scope to IEEE P3537 3Dblox work group



# **OUR INDUSTRY LEADERS**

### Si2 Board of Directors

Chair: Pankaj Kukkal Secretary: Leon Stok Treasurer: Lu Dai

NXP IBM Qualcomm Wilbur Lou Roger Carpenter James Culp Manoj Selva

Cadence Google GF Intel

Niels Faché Jung Yun Choi Mo Movahed Banghyun Sung

Keysight Samsung Siemens SK Hynix

Jacob Avidan Lluis Paris Gaurav Varshney Synopsys **TSMC** 

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### **Technology Steering Group**

Chair: Kerim Kalafala IBM Solaiman Rahim Synopsys Vivek Rajan Intel Aparna Dey Cadence Prabhas Kumar Ansys Narasimhan Narayan NXP Sorin Soimu Qualcomm Chris Mueth Keysight

### WGs & SIGs

### **UPM WG**

Chair: Nagu Dhanwada IBM

### **AIML Schema WG**

Chair: Ivan Kissiov

Siemens

ARM

### **AIML SIG**

Chair: Akilesh Kumar **Synopsys** 

### 3DIC SIGs

Chair: Rob Christy

### Coalitions

### **OpenAccess**

**BOD Chair: Ray Rodriguez** Intel BOD Rep: Haijun Fang **TSMC** BOD Rep: Diego Garcia Keysight BOD Rep: Yong Hwan Jeon SK Hynix BOD Rep: Zhiying Chen IBM Cadence CT Co-chair: Mark Rossman CT Co-chair: Adam Matheny IBM **ESG Chair: James Masters** Intel

### **Unified Power & Thermal**

Chair: Nagu Dhanwada IBM

### **Compact Modeling**

Chair: Peter Lee Micron Vice Chair: Jushan Xie Cadence Treasurer: Takeshi Naito Kioxia GF Secretary: Tanvir Morshed Model QA: Shahriar Moinian Broadcom

### Advisor: Geoffrey Coram **Analog Devices**

### **LLM Benchmarking**

Nathaniel Pinckney NVIDIA Igor Markov Synopsys



# MEMBER RECOGNITION

### The 2024 - 2025 Annual Power of Partnership (POP) Award

Peter Lee Micron
Shahed Reza Sandia I
Colin Shaw Silvaco
Gert-Jan Smit NXP

Micron Sandia Nat. Labs Silvaco NXP The POP award honors the organizing committee of the inaugural Si2 International Compact Modeling Conference (ICMC), held on June 26-27 in San Francisco. The ICMC is a collaborative platform that unites academic and industry stakeholders in sharing advancements in the development, application, and standardization of compact models for semiconductor devices. The committee successfully managed the logistical, administrative, financial, and programmatic requirements of the inaugural conference.

The 2024 – 2025 Quarterly Pinnacle Award			
Q3 '24	Daniel Cross	Cadence	For implementation of a single UPM model to represent and analyze power for an AMS system.
Q4'24	Jeff Wilson	IBM	For guiding definition of a translator to produce a human-readable format of OpenAccess data.
Q1 '25	Rudy Albachten	Intel	For a long list of contributions to the OpenAccess Coalition and chairing the oaScript workgroup.
Q2'25	Ivan Kissiov	Siemens	For significant contributions as AI/ML EDA SIG member and as AI/ML Schema OpenStandards WG chair.

# THE SI2 EXTENDED STAFF

### **Full Time Staff**



Robert Aslett CEO, President



Dr. Leigh Anne Clevenger Marshall Tiner **VP Technology** 



Sr. Director OA



Dr. Ali Sadigh Principle SW Des. Eng.



**Christy Pack** Sr. SW Design Engineer





Terry Berke Marketing Advisor



Jerry Frenkel Technical Advisor



Dr. Rhett Davis (NCSU) Technical Advisor



Jay Oak Technical Advisor



Alan LaRotonda PM Member Services



Marc Rose Exec Technical Asst.



Chris Falkowski Sr. SW Engineer



Carlo Barrientos **CAD SW Engineer** 



**Dominic Dimarco** SW Dev Engineer

# HOW OUR MEMBERS ENGAGE

Increasing Maturity

**Technology Steering Group** 

### **Special Interest Groups**

- Explore topics, influence peers
- Share knowledge within SIG
- Publish whitepapers

### **OpenStandards WGs**

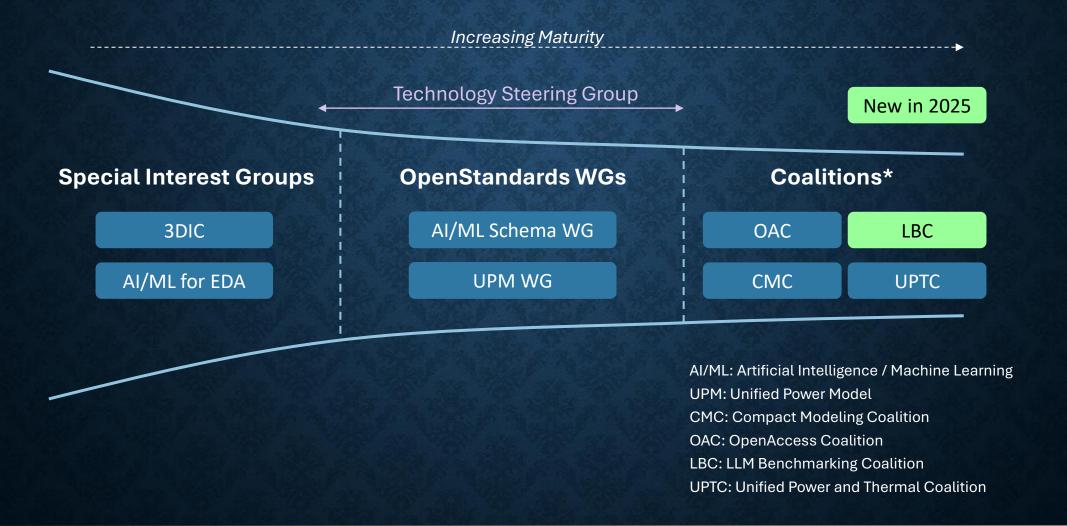
- Prototype solutions
- Prove value in member environment
- Share content within WG

### **Coalitions**

- Extend production solutions
- Continuously improve
- Share content within coalition
- Share content with public



# **OUR CURRENT PROGRAMS**





Coalition	Goal	Key Accomplishments
OpenAccess	Continuously improve the most widely used open reference design database	<ul> <li>oa22.61 code stream sunset (no additional changes)</li> <li>Released 22.61p013, 'p014, 'p015, 'p017, 'p019, 'p022, 'p024, 'p026</li> <li>New 22.62 Code Stream</li> <li>Functional change to oaParamArray class</li> <li>Will drive platform Matrix to RHEL 8.4, C++20</li> <li>Oa22.62p005 and oa22.63p009 released</li> <li>Extension Releases</li> <li>oaxColor 1.1 released 12/24</li> <li>oaScript 6.0 to support DM62 – In ESG review</li> <li>Polygon Operators 2.2 in test for September release</li> <li>Oa2json &amp; json2oa version 1.1 in test for September release</li> </ul>



Coalition	Goal	Key Accomplishments
	Continuously improve SPICE models that are the trusted foundation for R&D	<ul> <li>Successful International Compact Modeling Conference (ICMC) with 80 attendees, 3 distinguished keynote talks, 7 invited speakers, 23 oral presentations, and 16 posters across a two-day single track conference June 26 - 27 in downtown San Francisco.</li> </ul>
		<ul> <li>All papers now available on IEEE Xplore</li> </ul>
Compact		<ul> <li>ICMC Organizing Committee received Si2's Power of Partnership award</li> </ul>
Modeling		<ul> <li>Production model releases over the past 10 months: ASM-ESD, BSIM-BULK, BSIM4, BSIM-CMG, BSIM-IMG, BSIM-SOI, HiSIM_HV, MEXTRAM, PSP, OMI</li> </ul>
		<ul> <li>Si2 CMC is a sponsor for the International Conference on Simulation of Semiconductor Processes and Devices – SISPAD 2025 in Grenoble, France</li> </ul>
		Selection of two new standard models underway



Coalition	Goal	Key Accomplishments
Unified Power & Thermal	Enable adoption of UPM for fast & accurate IP/system level power analysis	<ul> <li>"Powering the Future: Mastering IEEE 2416 System-Level Power Modeling Standard for Low-Power AI and AMS Designs," tutorial presentation at DAC 2025, with presentations from UPTC member companies Cadence, IBM, NC State, Qualcomm, and Samsung, with over 25 attendees</li> <li>Completed Phase 2 Proof-of-Concept with Samsung using their technology, next focusing on dynamic power analysis</li> <li>Completed Phase 2 Proof-of-Concept with Qualcomm on system level power</li> <li>Welcomed Keysight as a new UPTC member</li> </ul>



Coalition	Goal	Key Accomplishments
New LLM Benchmarking	Expedite LLM development for semiconductor design	<ul> <li>Informational meetings and announcements at DAC and ICLAD led to successful kickoff meeting July 31 with 14 member companies/universities</li> <li>Press release to Business Wire on August 7</li> <li>Officers elected on August 14 <ul> <li>Nathaniel Pinckney, Nvidia, LBC chair</li> <li>Igor Markov, Synopsys, LBC vice-chair</li> </ul> </li> <li>Technical "Office Hours" and subgroups established for faster execution</li> <li>Open to new members – no fee in 2025, current OpenAccess &amp; Si2Base members pay no fee in 2026</li> </ul>



# **KEY 2024-2025 OSWG ACCOMPLISHMENTS**

WG	Goal	Key Accomplishments
AI/ML Schema for EDA	Enable vendor-agnostic algorithms & app development	<ul> <li>Ivan Kissiov, Siemens EDA, received Si2 Q2 Pinnacle award for service as group chair</li> <li>Arizona State University and Drexel University implemented use cases to illustrate pipeline of components to connect EDA to ML         <ul> <li>Ontology-&gt;Croissant-&gt;Data source-&gt;Communication layer</li> <li>Use cases: Net Length prediction, Arc delay predictor, Pre-route stage delay prediction, Timing prediction</li> </ul> </li> <li>Shared ontology for data organization and exchange used in test cases</li> <li>Unique agreement with Si2 funding universities to build on their work</li> </ul>

OSWG = OpenStandards Working Group



# **KEY 2024-2025 OSWG ACCOMPLISHMENTS**

WG	Goal	Key Accomplishments
		<ul> <li>"Powering the Future: Mastering IEEE 2416 System-Level Power Modeling Standard for Low-Power AI and AMS Designs," Tutorial presentation at DAC 2025, with new AMS demo from member companies Cadence and NC State</li> <li>This System-Level Power Demo showed how IEEE 2416 can aid in power</li> </ul>
Unified	Refine IEEE 2416 to	planning, sequencing, and architecting a complex mixed-signal system.
Power Model	support power models for complex designs	<ul> <li>Scenario generation and UPMPowerCalc also produced power traces with fine grained information about system power contributions and allow early refinement of power saving strategies</li> </ul>
		Si2 UPMPowerCalc software innovation supports System-Level Power Demo
		IEEE 2416 Standard revised and submitted for final release by EOY 2025



# **KEY 2024-2025 SIG ACCOMPLISHMENTS**

SIG	Goal	Key Accomplishments
		<ul> <li>SIG members provided inspiration for and participated in ICLAD 2025 panel, "Without chip foundational models AI-native EDA for SoC will fail," including Ivan Kissiov, Siemens EDA, Akhilesh Kumar, Ansys, and panel Moderator Rajeev Jain, Qualcomm</li> </ul>
AI / ML for	Explore The best way to apply AI and ML for chip	<ul> <li>Presentations to the SIG on the Comprehensive Verilog Design Problem (CVDP) Benchmarks and subsequent discussions on evaluating LLM quality led to establishment of the LLM Benchmarking Coalition</li> </ul>
EDA	design	Knowledge sharing on EDA foundational model publications and direction will result in a planned executive summary as a white paper
		<ul> <li>MLCAD paper, "Privacy-Preserving Data and Model Sharing for EDA via Inference Control and DP-SGD," Si2-mentored project at Center for Advanced Electronics Through Machine Learning (CAEML) by Ziyu Deng, NCSU</li> </ul>



# **KEY 2024-2025 SIG ACCOMPLISHMENTS**

SIG	Goal	Key Accomplishments
3D IC	Explore opportunities for standards and beneficial shared utilities for 3DIC	<ul> <li>Marc Rose, Si2, provides key inputs to the IEEE P3537 3Dblox work group</li> <li>3DBlox core connectivity: Provided ten written comments, recommendations, and questions. Work group agreed to consider two recommendations.</li> <li>3Dblox power and thermal feasibility analysis: Provided written comments. One comment, shared with Prof. Andrew Kahng, is that the feasibility analysis for power supports only DC analysis, not transient analysis. Work group recommended starting a tiger team on this topic of transient analysis.</li> <li>3Dblox common constraints syntax: Provided written comments on the 3Dblox common constraints syntax, a way to provide early design/manufacturing constraints information before tech files are available. The work group agreed to include a well-understood way to migrate a design from using these early constraints to using the actual design rules later.</li> </ul>





# <u>Si2</u>

A Not-for-Profit Membership Organization

Suppliers and users who innovate on trusted standards and share solutions that lower development costs and increase design productivity

