# Si2 DAC Events/2025

## *Advancing Semiconductor Design*

## *Presented by the Silicon Integration Initiative*

**June 22 and June 24 | Moscone West | San Francisco**

### *Tutorial -- Powering the Future: Mastering IEEE 2416 System-Level Power Modeling Standard for Low-Power AI and Beyond*

**Sunday, June 22, 9:00 - 12:30 PM | Moscone West, Room 3008**
**Register at www.dac.com**

### *IEEE 2416 System Power Modeling Working Group Open Meeting*

**Tuesday, June 24, 10:00 - 11:30 AM |Moscone West, Room 3016**
**REGISTRATION REQUIRED**

### *Panel -- Powering the Future of AI: Are Standards an Enabler or a Bottleneck?*

***Free Lunch for the First 50 Attendees***
**Tuesday, June 24, 12:00 - 1:00 PM | Moscone West, Room 3016**
**REGISTRATION REQUIRED**

### *Si2 OpenAccess Coalition Forum*

***Free Lunch for the First 50 Attendees***
**Tuesday, June 24, 1:00 - 2:45 PM | Moscone West, Room 3016**
**REGISTRATION REQUIRED**

### *Si2 Annual Member Meeting and Power of Partnerships Award Celebration*

**With a Presentation from NVIDIA**
**Followed by a Reception**
**Tuesday, June 24, 4:00 - 6:00 PM | Moscone West, Room 3016**
**For Si2 Members and Their Guests**
**REGISTRATION REQUIRED**

All meeting attendees must be registered for at least the “I Love DAC” level, which is available free **here** until June 9.

*Powering the Future*

# Mastering IEEE 2416 System-Level Power Modeling Standard for Low-Power AI and Beyond

**Sunday, June 22, 2025, 9:00 AM - 12:30 PM**
**Moscone West , Room 3008**
**Register at www.dac.com**

This tutorial will provide attendees with a comprehensive understanding of the IEEE 2416 standard, used for system-level power modeling in the design and analysis of integrated circuits and systems. Participants will gain practical knowledge necessary to implement and utilize the standard effectively. The tutorial will highlight the pressing need for low-power design methodologies, particularly in cutting-edge fields like AI, where computational demands are high. By getting a clear understanding of the IEEE 2416 standard, attendees will be equipped to make decisions on how the standard can be incorporated into their design flow to deliver the efficiencies needed to build their cutting edge low power designs. The presenters, who are experts from different industry segments (EDA, Foundry, SoC and IP) and academia who will use the IEEE 2416 standard positioned for a 2025 release.

## Agenda

- Introduction to IEEE 2416 and Power Modeling Evolution
- Core Concepts of IEEE 2416 – Digital and AMS Highlights
- Real-World Applications – Industry Deep Dives
- System-Level Example: AI Accelerator with AMS Blocks

## Who Should Attend

- IP Developers: Engineers responsible for designing and characterizing IP blocks who need to create accurate and efficient power models.
- SoC Architects and Designers: Professionals involved in system-level design and integration who require a deep understanding of power analysis and optimization using the 2416 standard.
- EDA Tool Providers and Users: Developers and users of EDA tools who integrate and leverage the capabilities of the 2416 standard in their workflows.

## Organizers

- Nagu Dhaswada, IBM
- Leigh Anne Clevenger, Si2

## Authors

- Daniel Cross, Cadence Design Systems
- Rhett Davis, NCSU
- Eunju Hwang,Samsung
- Tavares Forby, Qualcomm
- Akil Sutton, IBM

# IEEE 2416 System Power Modeling Working Group Open Meeting

**Tuessday, June 24, 2025, 10:00 - 11:30 AM**
**Moscone West , Room 3016**
**Complimentary Registration**

In the current dynamically changing landscape of computing, the growth of artificial intelligence (AI) applications has caused an exponential increase in energy consumption, re-emphasizing the need for managing power footprint in chip design.

To manage this escalating energy footprint and enable true system-level low-power design, modeling standards play a key role in facilitating interoperability and re-use. The IEEE 2416 system-level power modeling standard, introduced in 2019, offers a unified framework spanning system-level to detailed design, facilitating comprehensive low-power design for entire systems.This standard enables efficiency through contributor-based process, voltage, and temperature (PVT) independent power modeling.

The IEEE 2416 standard is currently positioned for a 2025 release with production industry-driven extensions in analog/mixed-signal, system modeling, and multi-voltage scenarios. Join this open meeting of the IEEE 2416 committee to learn how this new release will enhance system power modeling productivity for you and your company.

**Discussions Include**

- New features in IEEE 2416-2025
- Ballot pool feedback and associated actions
- Standardization schedule

**Organizer**

Nagu Dhanwada, Chair of IEEE 2416, IBM

**Advanced Registration is Required.**
**Click Here to Register**

# Powering the Future of AI: Are Standards an Enabler or a Bottleneck?

***Free Lunch for the First 50 Attendees***
**Tuesday, June 24, 12:00 - 1:00 PM**
**Moscone West, Room 3016**
**Complimentary Registration**

As AI workloads scale dramatically, power, thermal management, and reliability have emerged as critical concerns. Industry standards such as IEEE 2416 and IEEE 1801 have attempted to address these issues through system-level power and thermal modeling. But are these standards accelerating innovation, or have they become a bottleneck for rapid technological advancement?

Powering the Future of AI features panelists from industry leaders in design and methodology for power and thermal optimization, including IBM and Cadence Design Systems. The lunch forum includes experienced leaders in the semiconductor industry and EDA standardization and targets system designers and architects, logic and circuit designers, validation engineers, CAD managers, researchers, and academicians.

**Key Discussion Points**

- Standards: Foundation or Constraint to Innovation in AI and system-level power management?
- Practical impacts and industry adoption: Real-world experiences from semiconductor foundries, AI hardware developers, and system integrators.
- Bridging Gaps: The role of emerging IEEE 2416 extensions (A/MS, thermal, multi-voltage) in addressing AI workloads.
- Cross-industry perspectives from EDA tool vendors, system integrators, and IP developers.
- How should standards evolve to effectively enable next-generation AI applications?

**Panelists**

- Nagu Dhanwada, IBM, Moderator
- Sri Chilukuri, Arm
- Amit Srivastava, Synopsys
- Karan Sahni, Cadence Design Systems
- Rhett Davis, NCSU

**Advanced Registration is Required.**
**Click Here to Register**

# Si2 OpenAccess Coalition Forum

***Free Lunch for the First 50 Attendees***
**Tuesday, June 24, 1:00 - 2:45 PM**
**Moscone West, Room 3016**
**Complimentary Registration**

The OpenAccess Coalition Forum features innovations from industry experts, with topics ranging from ranging from curvilinear and 3D design to multi-threading performance improvements enabled by the OpenAccess API. Presenters from coalition member companies representing successful start-ups, international design companies, and academia, will discuss the strengths of OpenAccess technology and the value of membership.

**Who Should Attend**

- system designers and architects
- logic and circuit designers
- validation engineers
- CAD managers
- researchers and academicians

**Curvilinear Design and Application**
Aki Fujimura, CEO
Design 2 Silicon

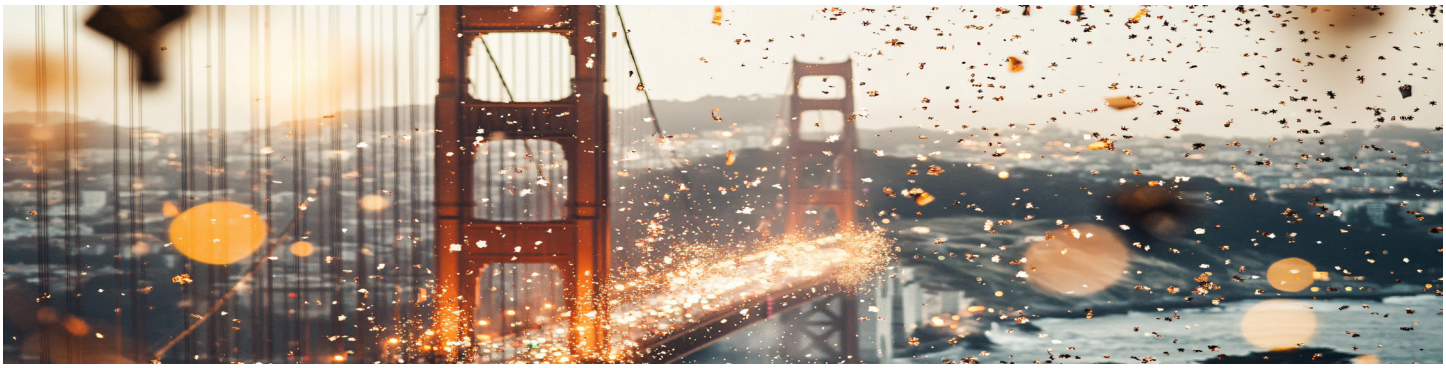
**How to Improve Performance and Connect with EDA Software Using the Open-Access API**
Yong-Hwan Jeon (Jason), CAD Engineer
SK-hynix

**An AI-Powered IC Routing**
Ed Grenert, Founder
Frontier Design Automation

**Fast Connectivity Highlighting with Polygon Operators Extension**
Simone Comensoli, Staff Software Systems Engineer
PDF Solutions

**Heterogeneous 3D Design with OpenAccess**
Rhett Davis, Professor
Electrical and Computer Engineering
NCSU

**Advanced Registration is Required.**
**Click Here to Register**



# Join Us at the Si2 Annual Member Celebration at DAC 2025

## *For Si2 Members and their Guests*

**Tuesday, June 24, 4:00 - 6:00 PM**

**Moscone West | Room 3016**

Join us for a celebration of collaboration at our annual members' meeting and reception. Gather with members, the board of directors, staff, and special guests as we toast to our joint achievements over the past year and see a sneak preview of our newest initiatives. Si2 will also present the annual Power of Partnerships Award.

The program will wrap up with a lively networking reception, where you can relax, connect, and share in the excitement with fellow DAC attendees.

### *Special Presentation by NVIDIA*

**Evaluation of LLMs for Si Design**
**Nathaniel Pinckney, Senior Research Scientist, NVIDIA**

**Hors D'oerves | Beer and Wine | Door Prizes**
**Admission is complimentary for Si2 members and their guests.**

**Advanced Registration is Required.**
**Click Here to Register**

# ICMC 2025

**International Compact Modeling Conference**

June 26-27, 2025 || The Clift Royal Sonesta, San Francisco

https://2025.si2-icmc.org/

The Compact Model Coalition (CMC) brings academia and industry partners together in the development and standardization of compact models for semiconductor devices. For 30 years now, the CMC has been instrumental in creating standardized and verified models for designers to use in their increasingly complex circuits for SPICE simulation.

The CMC is organizing a new and innovative International Compact Modeling Conference. Cosponsored by IEEE EDS, it will focus uniquely on compact device models, their development and broad application in the semiconductor industry. You are invited to participate in the evolution of these models, guide model development to help circuit designers create the best circuit performance possible, and enable foundries to leverage the strength of their device fabrication to full extent. Join the world experts in design, process technology, and model development to discuss state of the art semiconductor device modeling for a two-day in-person event in one location, offering a great opportunity to present and learn about this core element of circuit design and how to get the most from these global collaborations.


## THE CLIFT ROYAL SONESTA

***Book by May 26, 2025, to receive the reduced rate.***

Classic and contemporary with a nod to its storied past, The Clift Royal Sonesta San Francisco provides a wide array of amenities and services to make your stay comfortable.

495 Geary Street,
San Francisco, CA 94102

## KEYNOTE SPEAKERS

### Colin McAndrew

IEEE Life Fellow; NXP Fellow (retired);
ECpE; Iowa State University

### Keith Green

Texas Instruments; Distinguished
Member of the Technical Staff

### Sayeef Salahuddin

EECS, University of California, Berkeley;
TSMC Distinguished Professor and IEEE,
APS and AAAS Fellow

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