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# Nominee: Cadence Design Systems

**Representative: Aparna Dey**  
**Senior Product Marketing Group Director**

Aparna is a senior product marketing group director at Cadence, reporting to Cadence's Corporate vice president of Marketing. She is responsible for EDA and IP standards activities for Cadence and manages the participation, contribution, partnerships and relationships between Cadence and industry standards organizations, associations, alliances and consortium. She has more than 25 years of experience in EDA and system design industry in various leadership roles in R&D, design devices, technical marketing and system design. She has been at Cadence for over 16 years in various roles in R&D, services and technical marketing.



Prior to this role, Aparna was responsible for driving ASIC alliance partnerships and key technology deployments with leading customers at Cadence. She also led an incubator trans-national engineering group in Emerging Business Group responsible for design, development and support of an enterprise Silicon IP Reuse product. As a senior architect at Cadence Worldwide Services, Aparna has worked in multiple methodology projects on-site in Japan, Taiwan and Germany involving SOC chip integration, IP reuse, and DRAM design.

Aparna holds a bachelor's (B.E.) in Electronics and Telecommunication Engineering from Netaji Subhas Institute of Technology, University of Delhi, India.

From a standards perspective, Aparna has been deeply involved with various standards bodies like Si2, Accellera and IEEE and holds executive position in IEEE CEDA as VP of Standards and officer position in the IEEE DASC committee as the treasurer and secretary. She is also currently Board member and officer at Accellera and Si2. Aparna is passionate about Standards and is proud of her long association with Si2 executive team and staff since 2003 in various Si2 coalitions and committees. She hopes to help Si2 drive Standards to help EDA interoperability and foster growth of the ecosystem.

## **Nomination Statement: Cadence Design Systems**

Cadence is a pivotal leader in electronic systems design, building upon more than 30 years of computational software expertise. The company applies its underlying Intelligent System Design strategy to deliver software, hardware and IP that turn design concepts into reality. Cadence customers are the world's most innovative companies, delivering extraordinary electronic products from chips to boards to complete systems for the most dynamic market applications, including hyperscale computing, 5G communications, automotive, mobile, aerospace, consumer, industrial and healthcare.

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# Nominee: GlobalFoundries

**Representative: Richard Trihy, Vice President  
Design Enablement**

Richard is vice president of Design Enablement, GlobalFoundries. In this role Richard is responsible for the enablement and provision of PDKs, models and EDA design flows for GlobalFoundries customers and partners.

Prior to GlobalFoundries, he was director of R&D at Synopsys and group director R&D at Cadence Design Systems. He obtained B.E. and MEngSc degrees in Electrical Engineering from University College Cork, Ireland, and a Ph.D. degree in Electrical and Computer Engineering from Carnegie Mellon, Pittsburgh. Richard has led development teams in analog/mixed signal and RF design tools at Cadence where he represented Cadence on Verilog-A, Verilog-AMS and IEEE VHDL-AMS industry standards committees. At Synopsys, Richard led development teams in the Implementation Group and was founding chairman of the Si2 Liberty TAB.

With his broad background and over 20 years of experience in design methodology, semiconductor and EDA he will be able to contribute to the development of useful EDA standards.

## **Nomination Statement: GlobalFoundries**

GlobalFoundries is the world's first full-service semiconductor foundry with a truly global footprint. Launched in March 2009, the company has quickly achieved scale as one of the largest foundries in the world, providing a unique combination of advanced technology and manufacturing to more than 150 customers. With operations in Singapore, Germany and the United States, GlobalFoundries is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents.

The company's 300mm fabs and 200mm fabs provide the full range of process technologies from mainstream to the leading edge. This global manufacturing footprint is supported by major facilities for research, development and design enablement located near hubs of semiconductor activity in the United States, Europe and Asia. For more information, visit <http://www.globalfoundries.com>.



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# Nominee: Google

## **Representative: Roger Carpenter, Hardware Engineer**

Roger is a Google hardware engineer with more than years 30 of experience in electronic design automation and chip design.

Before joining Google, Roger held executive roles at three EDA firms: Magma Design Automation, Javelin Design Automation and Envis. His design experience includes positions at Wave Computing, Broadcom, Chromatic Research and Xilinx.

A holder of more than a dozen patents, Roger received a Bachelor's and Master's of Electrical Engineering and Computer Science from the Massachusetts Institute of Technology.

## **Nomination Statement: Google LLC**

Google LLC is an American multinational technology company that specializes in Internet-related services and products, which include online advertising technologies, search engine, cloud computing, software, and hardware. The hardware includes the Tensor Processing Unit (TPU which is an AI accelerator application-specific integrated circuit (ASIC) developed by Google specifically for neural network machine learning. Its headquarters are in Mountain View, California.



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# Nominee: IBM

## Representative: Leon Stok, Vice President, EDA

Leon is currently vice president of EDA at IBM and is responsible for delivering and supporting productive and effective design methodologies for all IBM design teams. This group develops design tools and design methods and provides both tools and supports experts to the entire silicon and system design community. Leon has a vision to take the CAD industry to platform level and sees a crucial role for Si2 to play in this evolution.

Prior to this he held positions as director of EDA, executive assistant to IBM's senior vice president of Technology and Intellectual Property and executive assistant to IBM's senior vice president of the Technology Group. Leon has been involved in the research and development of EDA tools for more than twenty years.

Leon studied electrical engineering at Eindhoven University of Technology, the Netherlands, from which he graduated with honors in 1986. He obtained a Ph.D. degree from Eindhoven University in 1991. Leon Stok worked at IBM's Thomas J. Watson Research Center as part of the team that developed BooleDozer, the IBM logic synthesis tool. Subsequently he managed IBM's logic synthesis group, and lead all of IBM's design automation research as the Senior Manager Design Automation at IBM Research from 1999-2004.

Leon has published over fifty papers on many aspects of high level, architectural and logic synthesis, low power design, placement driven synthesis and on the automatic placement and routing for schematic diagrams. He was elected an IEEE fellow for the development and application of high-level and logic synthesis algorithms. With a diverse background and a passion to develop efficient design platforms, he will be able to contribute strongly to the development and promotion of useful EDA standards.

## Nomination Statement: IBM

The systems and products designed by IBM rely heavily on the ability to quickly and accurately design complex silicon functions. Over the last decades the silicon content of IBM systems has increased drastically. This requires a significant improvement in designer productivity. Something that can only be realized by design tools that are operating in flows that are as seamless as possible our design flows consist of a mixture of internally developed and externally acquired tools from most EDA vendors. The interoperability of this entire toolset is essential to deliver the productivity required. Therefore, IBM is a strong supporter of open EDA standards and technologies and vigorously supports the objectives of Si2.



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# Nominee: Intel

**Representative: Rahul Goyal, Vice President and General Manager, Product and Design Ecosystem Enablement**

Rahul is Vice President and General Manager of Intel's product and design ecosystem enablement, including engagements, strategic alliances, sourcing, industry relations, ecosystem capability & infrastructure across Intel's broad product portfolio and for Intel Foundry Services. He and his team are responsible for the sourcing and licensing of software, semiconductor intellectual property (IP), electronic design automation (EDA), outsourced design services, and electronic measurement solutions used for product design, validation, and technology development.



During his 30+ year tenure, Goyal has held various technical and leadership roles in software engineering, technology development, planning, and business management. His previous roles include VP of EDA Business in the Design and Technology Solutions Group, Director of Intel's integrated silicon technology roadmap in the Microprocessor Products Group, and Senior Engineering Manager in Intel Mask Operations. Prior to Intel, Goyal was a hardware design engineer.

Goyal represents Intel on the Board of Directors of Silicon Integration Initiative (Si2), an R&D collaborative industry consortium focused on design interoperability standards development and adoption. He has served on the board of directors of several private technology companies since 2000, and was chairman of the Design Technology Council, an industry think tank, from 2007 to 2009. Goyal holds a Master's degree in Computer Engineering from Syracuse University in New York, and a Bachelor's degree in Electrical and Electronics Engineering (with honors) from Birla Institute of Technology and Science in Pilani, India.

## **Nomination Statement: Intel**

The systems and products designed by Intel Corporation rely heavily on the ability to quickly and accurately design complex silicon functions. Over the last ten years, not only has the silicon content of Intel systems increased exponentially, but a migration from a design environment of internally developed EDA tools to a large number of EDA tools acquired commercially has also occurred. Given that Intel subscribes to a multiple EDA vendor philosophy and uses a cross-section of tools from EDA vendors, the interoperability of those tools is essential for effective silicon design. Therefore, Intel is a strong supporter of open EDA standards and technologies and vigorously supports the objectives of Si2.



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# Nominee: Qualcomm Technologies

**Representative: Pankaj Kukkal**  
**Vice President of Engineering**

Pankaj is vice president of Engineering at Qualcomm Inc. In his current role, he oversees all EDA, emulation, post-silicon engineering and third party IP planning for mobile, compute, automotive, artificial intelligence/machine learning, and XR business units. He joined Qualcomm in 2012 and has contributed to delivering over 100 leading-edge SoCs in various application domains. Pankaj has more than 25 years of experience in EDA, silicon, systems, and software engineering.



Before joining Qualcomm, he held various leadership positions at Intel, focusing on CAD, emulation and validation. He has led the creation of several industry-leading technologies for chip design, emulation and post-silicon debug and automation.

Pankaj has a bachelor's degree in electrical engineering from the National Institutes of Technology, India, and a master's degree in computer engineering from the University of South Carolina.

Pankaj has lived in South Carolina, Oregon, Texas and California. In his free moments he enjoys his time with his wife and two daughters. He also likes skiing and boogie boarding, and he can do both in and around San Diego!

## **Nomination Statement: Qualcomm Technologies**

At Qualcomm, we invent breakthrough technologies that transform how the world connects, computes, and communicates. With a long-standing R&D focus, more than \$50 billion in cumulative research and development spend, over 130,000 patents and patent applications, and more than 30 years of innovation in chipsets, software, services and integrated platform solutions, we create foundational technologies that revolutionize the way people connect.

For decades, Qualcomm has helped enable the entire mobile ecosystem and powered many of your smartphone's capabilities. We were instrumental in driving the development and launch of 3G and 4G. Now, we're building upon that history of technology leadership as we do the same with 5G, which will have a significantly greater impact than previous generations. 5G serves as the foundational technology that makes it possible for everything and everyone to communicate and interact seamlessly, across connected cars and industrial IoT, smart homes and smart cities, networking and mobility. Qualcomm continues to break new ground, innovating across multiple technologies such as CPU, GPU, modem, GPS, connectivity, etc., and as a result is continually expanding our product offerings.

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# Nominee: Samsung Electronics

**Representative: Dr. Jung Yun Choi, Corporate Vice  
President, Electronics Design Technology Team**

Jung Yun is corporate vice president for the Samsung Electronics Design Technology Team. A 19-year Samsung veteran, Jung Yun leads the technology team responsible for developing all design infrastructure, PDK, DK, tools and methodologies for Samsung memory products, technologies and environments impacting product values, new process and package technologies, new applications and working environments.

Since joining Samsung, he has contributed to the development of low-power design methodologies for mobile SoC in Samsung SLSI business, RTL-to-GDS implementation and sign-off methodologies for customers in Samsung foundry business, and PDK/DK and in-house tools for DRAM/Flash products in Samsung memory business.

Jung Yun joined Samsung Electronics in 2003 after receiving his doctorate in Electrical Engineering at the Pohang University of Science and Technology, Republic of Korea. He was also a visiting scholar at Stanford University in 2012.

## **Nomination Statement: Samsung Electronics**

The Samsung Electronics Device Solutions Division has three semiconductor Business Groups: Memory Business, SLSI Business, and Foundry Business. We need to prepare a seamless design flow with diverse tools from different EDA vendors for not only internal designs (Memory and SLSI) but also outside customers (Foundry).



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# Nominee: Siemens EDA

**Representative: Anant Adke**  
**Vice President of Engineering**

Anant is the vice president of Engineering in the Calibre group of Siemens EDA (formerly Mentor Graphics). His teams develop high-performance, compute-intensive software addressing the physical verification needs of the semiconductor industry's leading-edge nodes. He joined Mentor in 1995.

During his tenure at Calibre, Anant has managed engineering groups responsible for implementing interfaces to industry standard design creation tools and databases such as OpenAccess and represented Mentor Graphics on the OpenAccess Coalition.

Anant holds a bachelor's degree in electrical engineering from Indian Institute of Technology Bombay, and a master's degree in computer engineering from University of Michigan, Ann Arbor.

## **Nomination Statement: Siemens Digital Industries Software**

Siemens Digital Industries Software is a world leader in electronic and software design solutions, providing products, consulting services, and award-winning support for the world's most successful electronic, semiconductor and systems companies. We are unique in providing solutions for both the hardware components (the chips and boards) and the software components (the embedded operations systems and applications/drivers that control the product's operation). Since its inception, the company has focused on providing leading tools for the design and verification of electronic systems with a focus on best-in-class solutions. Siemens Digital Industries Software strongly promotes open design flows that enable our customers to build flows combining best-in-class products. The interoperability of EDA tools and the support of open EDA standards have been central to this mission.





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# Nominee: SK hynix

**Representative: Changho Do, Vice President  
Computer Aided Engineering Division**

Changho has been the head of SK hynix's Computer Aided Engineering Division since December 2019. Prior to that, he was as vice president of Strategy & Planning in the DRAM Development Division. He majored in physics at Kyungpook National University in South Korea and graduated from his BA in 1996.

Changho began working in the design team of SK hynix Memory Research Center in 1996. He worked as a circuit design engineer for memory product development. From 2005 to 2013, he worked as a project leader in memory design. Starting in 64M SDRAM development, Changho contributed to the development of the world's first DDR3 product. He was also in charge of the organization dedicated to the development of Analog IP for Memory for a certain period of time. He was elected to the CEO office in 2013, and in 2016 he served as the team leader directly supporting the CEO of SK hynix.



Changho was awarded the Industrial Service Medal from the Korean government in 2008 for his contributions to the industrial development of Korea. Currently, he holds more than 70 US patents related to the low power and high speed scheme, reliability and yield enhancement, and DFT/DFP in the field of memory design.

## **Nomination Statement: SK hynix**

SK hynix is a leading semiconductor company that produces DRAM, NAND flash memory semiconductors and CIS non-memory semiconductor products, and has solidified its technological leadership by introducing innovative products with the world's first-minimum-fastest-lowest voltage to the market.

The emergence of new digital products and the expansion of the IoT environment are gradually expanding the area and demand of semiconductors, and the and mobilization of IT devices demands more advanced semiconductor characteristics. To satisfy the characteristics of such advanced semiconductors, it is very important to design semiconductors quickly and accurately.

Semiconductor design requires the proper use of design tools provided by EDA vendors and internally developed (in-house) tools at each design stage, so compatibility between them is essential for efficient design. For this compatibility technology, SK hynix has introduced OA, the open EDA standard technology of Si2, and is continuously using and expanding it in internally developed tools. Therefore, SK hynix is actively supporting Si2's open EDA standards and technologies and is willing to provide leading support.

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# Nominee: Synopsys

**Representative: David DeMaria, Chief of Staff to President and COO**

Dave joined Synopsys in 2013 and is Chief of Staff to the President & COO, Sassine Ghazi. He has more than 25 years of experience in the EDA, IP and semiconductor industries. Prior to Synopsys, he held senior executive positions at Cadence, MoSys, Apache, Optimal, Viewlogic and Zuken. Dave attended Boston University for a B.S. degree in Computer Engineering.



## **Nomination Statement: Synopsys**

Synopsys, Inc. provides products and services that accelerate innovation in the global electronics market. As a leader in EDA, semiconductor intellectual property (IP) and Software Security, Synopsys' comprehensive, integrated portfolio of system-level, IP, implementation, verification, manufacturing, optical and field-programmable gate array (FPGA) solutions help address the key challenges designers face such as power and yield management, system-to-silicon verification and time-to-results.

These technology-leading solutions help give Synopsys customers a competitive edge in quickly bringing the best products to market while reducing costs and schedule risk. For more than 30 years, Synopsys has been at the heart of accelerating electronics innovation with engineers around the world having used Synopsys technology to successfully design and create billions of chips and systems.

The company is headquartered in Mountain View, California, and has over 100 offices located throughout North America, Europe, Japan, Asia and India. Synopsys continues to champion customers' requirements for interoperability throughout the EDA and semiconductor industries. Synopsys has made strong and valuable contributions of technology, manpower, and funding to a variety of organizations and initiatives that have resulted in tangible benefits to the design community.

Synopsys desires to continue its involvement with Si2 as a member of the Si2 Board of Directors to serve the electronics community by bringing expertise and resources to bear upon the ongoing challenge of interoperability for IC design and manufacturing. Synopsys agrees with Si2 that through collaborative efforts, the IC industry can achieve higher levels of SoC integration, improve productivity, and reduce costs.

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# Nominee: Texas Instruments

## **Representative: Keith Green, Distinguished Member of the Technical Staff**

Keith Green is a Distinguished Member of the Technical Staff at Texas Instruments in Dallas, Texas. During his 28 years with TI he has had various technical and leadership roles that spanned the fields of semiconductor modeling, reliability and technology development. Presently, he works in TI's Analog Technology Development department and is responsible for Hall-effect magnetic sensor technology.

Keith was a founder of the Compact Model Council consortium in 1996 and served as its chairman from 2012 to 2015. He guided strategic university research as chairman of the Semiconductor Research Corporation's Compact Modeling Technical Advisory Board from 2004 to 2011. He has served on the board of Silicon Integration Initiative since 2015.

Keith has 20 patents, over 20 publications, and has been an invited speaker at several conferences and universities. He received Ph.D. and M.S. degrees in Electrical Engineering from the University of Florida and a B.S. degree in Electrical Engineering from the University of Delaware.

## **Nomination Statement: Texas Instruments**

Texas Instruments Incorporated (TI) is a global semiconductor design and manufacturing company that develops analog integrated circuits and embedded processors. The process of designing these products relies heavily on electronic design automation tools. The accuracy of these tools is as critical as their ability to operate reliably with technology design kits developed both in-house and by commercial foundries. Therefore, TI has a strong interest in the mission of Si2 to deliver standards for improving IC design capability. As an integrated device manufacturer, TI's interests span manufacturing, design, packaging and test. As a member of the board of directors, TI would bring perspective on all of these aspects for a wide spectrum of technologies that include silicon for low-power to high-voltage, gallium-nitride, MEMs and sensors.

