## The Software Standard

## Industry Update: On Qualcomm & EDA

Much of the technical and end-markets commentary at the Qualcomm analyst meeting was, by implication, of particular relevance to the EDA companies, whose software enables the semiconductor industry; in addition, the trends commentary around cloud and industrial IoT was of direct or indirect relevance to a number of our other non-EDA companies, including Microsoft and PTC.

Among the more than 25 companies we track for our semiconductor R&D spending reviews, Qualcomm has the second-largest amount (behind Intel and ahead of AMD and Nvidia) and it is likely among the largest spenders for commercial EDA. Qualcomm has been among those companies (as we showed in our September 9th, 2021 industry report and in Chart 1a below) which has had an inflection in its R&D spending. As we show below in the section on open engineering positions, Qualcomm is, as might be expected, a consumer of multiple software and hardware products from the largest EDA companies.

Among the terms and concepts that were noteworthy and relevant were "one technology roadmap", "center of gravity of AI processing is moving to the edge", automotive "digital chassis", and "on-device intelligence", among others, from which a direct can line be drawn to EDA.

While we would not attempt to forecast the magnitude of revenue effects, the details of the Qualcomm technology roadmap, as described at the meeting, have implications for such principal EDA categories as synthesis, sign-off, simulation, verification, implementation, IP, EDA hardware, silicon lifecycle management, and software security (i.e., Synopsys' Software Integrity business vis-à-vis automotive, edge computing, and industrial IoT). What's interesting to consider is that semiconductor companies sound increasingly like systems companies, and systems companies (e.g., Apple, Microsoft) sound increasingly like semiconductor companies. The essentialness of EDA companies' role becomes only more apparent in this context of the customers' "arms races".

The (recorded) cameo appearance by Microsoft's CEO employed what for us has been a critical strategic concept for and about Microsoft, and an essential part of our investment thesis, namely "ubiquitous computing and ambient intelligence" (or UCAI, which we have referred to in numerous company reports). The Qualcomm technology roadmap might be considered (at least by us) as a subset of that broad UCAI concept (hence the company to company alignment). Microsoft itself has been investing heavily in its own proprietary silicon development.

Separately, see too our comments below on a recent technical presentation by Qualcomm at an Si2 industry event on the important subject of design data management.



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## **Companies Mentioned**

<u>Ticker</u>	<u>Price</u>	Rating
ANSS	\$399.36	Buy
CDNS	\$187.74	Buy
MSFT	\$339.12	Buy
PTC	\$119.64	Buy
QCOM	\$183.54	Not rated
SNPS	\$353.92	Buy

Aside from EDA effects, which is most of what we took away from the meeting, the commentary about "industrial IoT" is of most relevance (if perhaps indirectly) within the remainder of our Engineering Software group to PTC (industrial IoT necessitates compiling a complex ecosystem of applications development, analytics, data collection, connectivity, data storage, industrial automation, and local computing).

Separately, at an event hosted recently by the Si2 industry (on the launch of its *Titan* initiative), Qualcomm gave a presentation titled "*VLSI data in AI-ML/Auto/Cloud/Design*", the subject of which was very much aligned to our comments on the important role, prospectively, of a "unified data platform" for EDA (e.g., in the context for example of unifying Cadence's various verification stacks, or, as well, for IP design- and data-management). The main theme of the presentation was "data management challenges" facing EDA (that is, its customers), which was in effect the theme of our October 17th, 2021 report on EDA-PLM convergence.

The "emerging verticals driving new VLSI workflows" were shown as "EDA on cloud/hybrid compute setup", "Al/ML in VLSI data-driven design", "automotive long-tail support", and "custom ASICs & IoT multi-source IP". What Qualcomm proposed as a solution is complete design information and results in "one place", i.e., a design database plus APIs (this describes what is one of the most important architectural/technical paths occurring in the other half of Engineering Software, i.e., microservices plus APIs, albeit not by all of the major vendors).

#### SELECTED QUOTES FROM THE ANALYST MEETING - AND OUR COMMENTS

- "We are the company that will power the connected intelligent edge". We won't comment on how categorically correct or likely this, but, in EDA terms, the general direction of the trend will be enabled by analog/mixed-signal design tools (i.e., custom IC), i.e., Cadence, power analysis & optimization, i.e., Ansys, and possibly semiconductor IP (e.g., data plane, interface), i.e., both Synopsys and Cadence;
- "And what is unique about our model is that we have one technology road map that is scaled to address all growth vectors", The term "one technology roadmap" was referred to often (we haven't come across many companies multiple roadmaps for the same business, a roadmap may consist of multiple elements, or what Ansys refers to as "principles" in its technology strategy statement): in EDA terms this would suggest a steady building out of consistent design flows; and then -
- "Our mobile heritage and DNA put us in incredible position to provide high-performance, low-power computing, on-device intelligence, everything wireless and the leadership across not only AI processing, connectivity, but camera, graphics, hidden sensors, will scale to support every single device at the EDGE". We won't comment on the "incredible" part but in technical terms this was perhaps the most comprehensive statement that pertains to our software companies that sell to, partner with (Microsoft) or otherwise participate in the wider ecosystem or end-market trends (PTC). "Everything wireless" means Cadence and Ansys, "low-power" means Ansys (at least), and "connectivity"-"camera"-"sensors" likely means various semiconductor IP...;
- \*....we believe the future of the PC SoCs are going to be a fully integrated SoC. So I think that, that's something really important to understand. And so that means you're integrating CPU, GPU, all of these accelerators, connectivity, and so forth. That's all being integrated into one thing, one compute platform. And so for us, what that means is that we need to have a best-in-class CPU. And so I'm sure you're aware of us acquiring NUVIA. And so they're designing the next-generation Qualcomm CPU". All of the aforementioned "integrating" multiples the need for "verification", which entails a variety of EDA software tools and quite will also entail the consumption of hardware-based verification, including emulation and prototyping (e.g., for software bring-up). Over the past number of years, hardware has become a more than \$700 million business for the EDA Big 3 combined.

Similarly, the company's comment that, "software actually is the single most -- or area of highest growth, I would say, from a technology perspective. So a lot of spend going into software" also implies growing demand for products such as Cadence's Palladium and Protium, Siemens EDA's Veloce and Synopsys' Zebu and HAPS, for the purpose of hardware/software co-design and co-verification.

• "....The car is going to be connected to the cloud 100% of the time. With 5G, the car is connected to the cloud and when that happens, the car becomes a center of distribution of media, gaming, personalized experience, a lot of data analytics and artificial intelligence". The combination of connectivity-high data rates-internal networking-local computing implies multiple EDA requirements or usages, such as custom IC (e.g., analog/mixed-signal), simulation-analysis-verification (e.g., electromagnetics/RF, electrothermal), and quite possibly too Synopsys' newly created category of silicon lifecycle management (SLM).

And the cloudiness part of it should in principle be a plus for Microsoft in particular, given their industry alignment generally and the alignment with Qualcomm specifically ("few companies are as strategically aligned with Qualcomm as Microsoft. This is a very long-term relationship for Qualcomm").

In that regard it's important to keep in mind that Cadence and Synopsys have in just the past few years have become quite conscientious about the automotive market (where previously the technology complexity and volumes were deemed to be not very interesting). To its credit, Mentor (when it was still Mentor) established an automotive business years ago based on its cabling/wiring harness tools (likely *one* of the factors that led Siemens to be interested).

## **QUALCOMM RÉSUMÉS**

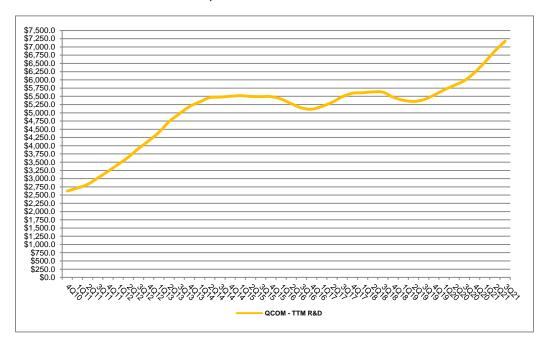
We undertook an initial spot check of Qualcomm's "engineering" open jobs data for references pertaining to EDA company names, brands and technologies, etc. which yielded the following (a baseline for future checks). There were of this date more than 1,580 engineering openings (as compared with about 2,900 at Intel). The references to specific EDA products suggest, as might be expected, that Qualcomm uses tools from Ansys, Cadence, and Synopsys.

- "ADAS", 74 references;
- "Allegro", 13. Allegro is Cadence's PCB brand (the second-largest by revenue in the PCB category, after Mentor's). A related search of "PCB" yielded 80 references, e.g., "system in package (SIP) design engineer, senior";
- "AR/VR", 116 references;
- "Automotive", 286 references;
- "Calibre", 6. Calibre is Siemens EDA's flagship physical verification product family and the largest by revenue in the physical verification category;
- "CPU", 240 references, more than half of which has to do with "physical design", i.e., a positive implication for the use of tools such ICC/Fusion and Innovus;
- "DRC", 28, e.g., "physical design engineer for mixed-signal ASICs", and "LVS, 24;
- "Emulation", 123, e.g., "validation/emulation engineer system/platform post-silicon"; "post-silicon & emulation CPU validation and debug". A related search of "prototyping" yielded more than 65 references;

• "Foundry", 47, e.g., "device engineer, semiconductor foundry (Hsinchu)", "silicon process technology & foundry engineer" (Hsinchu);

- "Genus" (Cadence's synthesis brand), 19;
- "GPU", 208, e.g., "Graphics (GPU) design implementation engineer" (Cork), "graphics (GPU) silicon validation/debug specialist", "GPU high-level modeling", "VR/AR architecture", "GPU software engineer", etc..
- "HAPS", 0 (HAPS is Synopsys' prototyping hardware brand, the largest by revenue in the categrory);
- "HFSS" (Ansys' electromagnetic simulation brand), 16, e.g., "principal 5G/RF-IC SiP/package design engineer",
- "IC Compiler" ("ICC"), 39, and "Fusion Compiler", 8. Fusion Compiler, the successor to ICC, is Synopsys' flagship physical implementation brand;
- "IC Validator" ("ICV"), 1. ICV is Synopsys' physical verification signoff brand;
- "Innovus", 28. Innovus is Cadence's physical implementation brand;
- "*loT*", more than 205 references;
- "Layout", 160 (including references to analog/RF layout and mask layout);
- "ML", more than 140 references, e.g., "ML/AI processor designer", "autonomy and ADAS R&D systems engineer";
- "Pegasus" (Cadence's physical verification brand), 0;
- "Palladium", 6;
- "*Primetime*" (Synopsys' timing-optimization brand), 50;
- "Protium" (Cadence's prototyping hardware brand), 1;
- "Redhawk" (Ansys' flagship power-optimization signoff brand), 8;
- "Synthesis", 193 (including more than 40 having to do with CPU synthesis). A related search for "RTL" yielded more than 245 references;
- "Tempus" (Cadence's timing-optimization brand), 19;
- "VCS" (Synopsys' RTL simulation brand), 22;
- "Veloce" (Mentor's hardware-based verification brand), 6;
- "Virtuoso", 35. Virtuoso is Cadence's custom IC (analog/mixed-signal) brand;
- "Voltus" (Cadence's power-optimization brand), 5; and,
- "Zebu", 3.

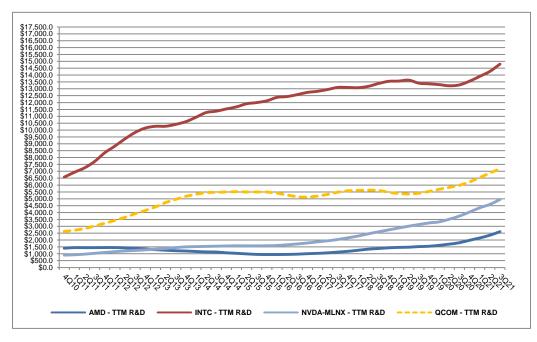
Chart 1a. Qualcomm TTM-R&D, calendar 2010-3Q21



Source: Company data, Griffin Securities.

Chart 1a comments. For the TTM ended 3Q21 (FY21), Qualcomm's R&D spending was \$7.175 billion, up 20% (vs. 11% in FY20 and down 4% in FY19). R&D in 4QFY21 was \$1.878 billion, up 19%. There has been a clear upward inflection as compared with the declines for the calendar periods ended 4Q18, 1Q19, 2Q19, and 3Q19.

Chart 1b. AMD--Intel-Nvidia-Qualcomm TTM-R&D, calendar 2010-3Q21



Source: Company data, Griffin Securities.

**Chart 1b comments.** As this report was being completed, Nvidia reported 3QFY22 R&D of \$1.403 billion, up 34% year/year and \$158 million sequentially, resulting in TTM-R&D of \$4.95 billion, up 41%.

Chart 2. Qualcomm, "industry trends"



Source: Qualcomm 2021 investor day.

**Chart comments.** These trends are not necessarily unique to Qualcomm, but many are of specific relevance to (indeed enabled by) EDA – "5g expands into enterprise networking", "Al gains scale at the edge", "digital chassis becomes the key asset in automotive" - <u>plus</u> direct or indirect relevance to companies such as Microsoft (e.g., "gaming moves to the cloud") and PTC (i.e., industrial IoT).

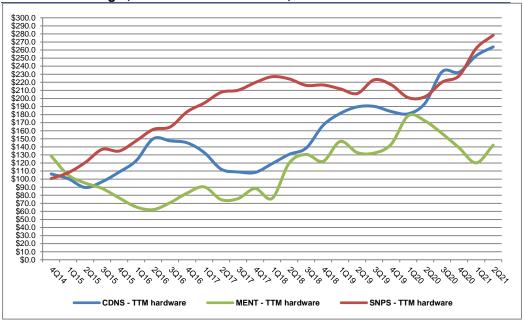
Chart 3. Qualcomm, CPU development



Source: Qualcomm 2021 investor day.

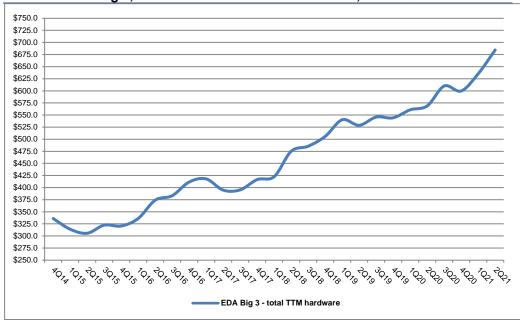
**Chart 3 comments.** Not unlike Apple's silicon development generally, or its M-series specifically, the Qualcomm CPU development ought to result in similar incremental EDA consumption.

Chart 4a. EDA Big 3, hardware TTM revenues, 2014-2Q21



Source: Company data, Griffin Securities.

Chart 4b. EDA Big 3, combined hardware TTM revenues, 2014-2Q21



Source: Company data, Griffin Securities.

Chart 4a-4b comments. The growth in the EDA hardware category in recent years has been driven by both semiconductor and systems customers. In the most recently available TTM data (for the period ended 2Q21), Synopsys had the largest amount of hardware revenues, followed by Cadence, then Siemens.

### Chart 5a. Qualcomm, design data management (1)

# Data Management Challenges

Qualcom

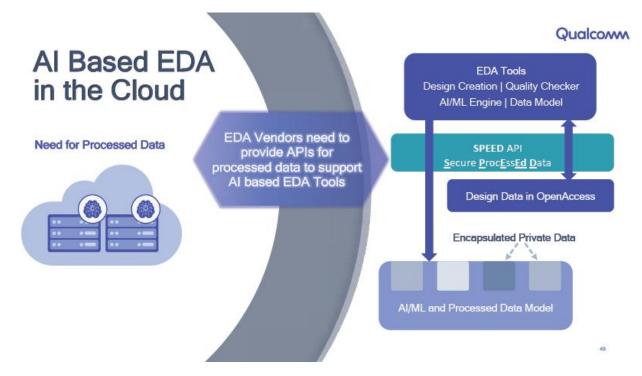
Goal: Streamline data collection, completeness, processing, optimize volume and usable over time

Complete and Efficient	Need single source of data capturing complete design/setup/results/metrics  - Currently distributed between multiple EDA tool databases, side files, scripts, reports  Standardize fundamental file formats  - Continuous effort of parsing generated files and reports for analytics, design closure  - Basic reports for Timing/DRC/Formal in proprietary formats, delay decisions/ML/debug
Data Volume	Standardize data for efficient storage and mining  - Currently distributed in multiple formats with overlapping information but none complete (Design information of connectivity, timing, power, physical information is distributed in Verilog, DEF, GDS, SPEF, OA, STA sessions, PDN database, P&R databases and internal formats)  - Reduce terabytes of duplicate data by defining a standard dataset for Al/ML, cloud transfers and ability to reproduce and debug for Auto
Reproduce and Debug over time	Interface Standards for integration and debug over time  - High risk for mission critical debug as EDA Database is binary version specific and need to bring up with same hidden tool options, defaults.  - IoT and custom ASSP designs need IP protection. Develop standard API for integration and EDA debug

<sup>\*</sup> DEF : Design Exchange format, SPEF : Standard parasitic exchange format, STA ; static timing analysis; PDN : Power distribution network, P&R; Place and Route

Source: Qualcomm, Si2, November 4, 2021

Chart 5b. Qualcomm, design data management (2)



Source: Qualcomm, Si2, November 4, 2021

**Chart 5a-5b comments.** The solution to the proposal by Qualcomm could be one or both of internal work by the EDA vendors and/or close connection to a relevant PLM platform (from the specifications described by Qualcomm

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#### **COMPANIES MENTIONED:**

Ticker	Company Name	Rating
ANSS	Ansys, Inc.	Buy
CDNS	Cadence Design Systems Inc.	Buy
MSFT	Microsoft Corp.	Buy
PTC	PTC Inc.	Buy
QCOM	QUALCOMM Inc.	Not Rated
SNPS	Synopsys Inc.	Buy

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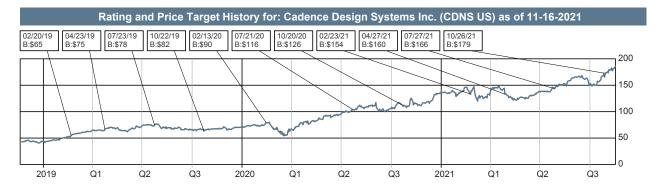
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