
Nominee: Ansys, Inc.

Representative: John Lee, General Manager and Vice President, Ansys Electronics and Semiconductor Unit

John Lee is general manager and vice president of the Ansys Electronics and Semiconductor Unit.

He co-founded and served as CEO of Gear Design Solutions, which was acquired by Ansys in 2015. Gear Design developed the first purpose-built big data platform for integrated circuit design. Lee had previously co-founded Mojave Design, which was acquired by Magma Design Automation and later purchased by Synopsys in 2012. His first startup, Performance Signal Integrity, was acquired by Avanti, and then by Synopsys.



Nomination Statement: Ansys, Inc.

Ansys develops, markets and supports engineering simulation software used to predict how product designs will behave in real-world environments ranging from a rocket launch, flying an airplane, driving a car, using a computer, touching a mobile device, crossing a bridge, or putting on a wearable technology.

For semiconductor and electronic systems design, compute-intensive pervasive simulation coupled with machine learning is critical to solve multi-physics challenges of power, performance, thermal, variability, timing, electromagnetics, h/w security and reliability challenges across multiple domains of chip-package, and system (CPS). The phases of product ideation, design validation, manufacturing, deployment to product life cycle management require an eco-system of partners, and interoperability standards, especially as we move to 5nm and below technology nodes, to ensure time to results and PPA goals. Ansys believes in collaboration, competencies and commitment of partners to enable customer success and supports the mission of Si2.

Nominee: Cadence Design Systems

Representative: Aparna Dey
Senior Product Marketing Group Director

Aparna Dey is a senior product marketing group director at Cadence, reporting to Cadence's Corporate vice president of Marketing. She is responsible for EDA and IP standards activities for Cadence and manages the participation, contribution, partnerships and relationships between Cadence and industry standards organizations, associations, partnerships and consortium. She has more than 25 years of experience in EDA and system design industry in various leadership roles in R&D, design services, technical marketing and system design. She has been at Cadence for over 16 years in various roles in R&D, methodology services and technical marketing.



Prior to this role, Aparna was responsible for driving ASIC alliance partnerships and key technology deployments with leading customers at Cadence. She also led a multi-national incubator engineering group in Emerging Business Group at Cadence to drive engineering development, deployment and support of an enterprise Silicon IP Reuse management product and solution. As a senior architect in Cadence Worldwide Services, Aparna has worked in multiple methodology projects on-site in Japan, Taiwan and Germany involving SOC chip integration, IP reuse, and DRAM design.

Aparna holds a bachelor's (B.E.) in Electronics and Telecommunication Engineering from Netaji Subhas Institute of Technology, University of Delhi, India.

From a standards perspective, Aparna has been deeply involved with various standards bodies like Si2, Accellera and IEEE and holds board and officer positions in Accellera, Si2 and IEEE DASC committee. Aparna is passionate about Standards and is proud of her long association with Si2 executive team and staff since 2003 in various Si2 coalitions and committees. She hopes to help Si2 drive Standards to help EDA interoperability and foster growth of the ecosystem.

Nomination Statement: Cadence Design Systems

Cadence is a pivotal leader in electronic design, building upon more than 30 years of computational software expertise. The company applies its underlying Intelligent System Design strategy to deliver software, hardware and IP that turn design concepts into reality. Cadence customers are the world's most innovative companies, delivering extraordinary electronic products from chips to boards to systems for the most dynamic market applications, including consumer, hyperscale computing, 5G communications, automotive, mobile, aerospace, industrial and healthcare.

Nominee: GLOBALFOUNDRIES

Representative: Richard Trihy, Vice President of Design Enablement

Richard Trihy is vice president of Design Enablement, GLOBALFOUNDRIES. In this role Richard is responsible for the enablement and provision of PDKs, models and EDA design flows for GLOBALFOUNDRIES customers and partners.

Prior to GLOBALFOUNDRIES, he was director of R&D at Synopsys and group director R&D at Cadence Design Systems. He obtained B.S. and M.S. degrees in Electrical Engineering from University College Cork, Ireland, and a Ph.D. degree in Electrical and Computer Engineering from Carnegie Mellon, Pittsburgh. Richard has led development teams in analog/mixed signal and RF design tools at Cadence where he represented Cadence on Verilog-A, Verilog-AMS and IEEE VHDL-AMS industry standards committees. At Synopsys, Richard led development teams in the Implementation Group and was founding chairman of the Si2 Liberty TAB.

With his broad background and over 20 years of experience in design methodology, semiconductor and EDA he will be able to contribute to the development of useful EDA standards.

Nomination Statement: GLOBALFOUNDRIES

GLOBALFOUNDRIES is the world's first full-service semiconductor foundry with a truly global footprint. Launched in March 2009, the company has quickly achieved scale as one of the largest foundries in the world, providing a unique combination of advanced technology and manufacturing to more than 150 customers. With operations in Singapore, Germany and the United States, GLOBALFOUNDRIES is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents.

The company's 300mm fabs and 200mm fabs provide the full range of process technologies from mainstream to the leading edge. This global manufacturing footprint is supported by major facilities for research, development and design enablement located near hubs of semiconductor activity in the United States, Europe and Asia. For more information, visit <http://www.globalfoundries.com>.



Nominee: Google

Representative: Roger Carpenter, Hardware Engineer

Roger Carpenter is a Google hardware engineer with more than years 30 of experience in electronic design automation and chip design.

Before joining Google, Roger held executive roles at three EDA firms: Magma Design Automation, Javelin Design Automation and Envis. His design experience includes positions at Wave Computing, Broadcom, Chromatic Research and Xilinx.

A holder of more than a dozen patents, Roger received a Bachelor's and Master's of Electrical Engineering and Computer Science from the Massachusetts Institute of Technology.



Nomination Statement: Google LLC

Google LLC is an American multinational technology company that specializes in Internet-related services and products, which include online advertising technologies, search engine, cloud computing, software, and hardware. The hardware includes the Tensor Processing Unit (TPU) which is an AI accelerator application-specific integrated circuit (ASIC) developed by Google specifically for neural network machine learning. Its headquarters are in Mountain View, California.

Nominee: IBM

Representative: Leon Stock, Vice President, EDA

Dr. Leon Stok is currently vice president of EDA at IBM and is responsible for delivering and supporting productive and effective design methodologies for all IBM design teams. This group develops design tools and design methods and provides both tools and supports experts to the entire silicon and system design community. Leon has a vision to take the CAD industry to platform level and sees a crucial role for Si2 to play in this evolution.

Prior to this he held positions as director of EDA, executive assistant to IBM's senior vice president of Technology and Intellectual Property and executive assistant to IBM's senior vice president of the Technology Group. Leon has been involved in the research and development of EDA tools for more than twenty years.

Leon studied electrical engineering at Eindhoven University of Technology, the Netherlands, from which he graduated with honors in 1986. He obtained a Ph.D. degree from Eindhoven University in 1991. Leon Stok worked at IBM's Thomas J. Watson Research Center as part of the team that developed BooleDozer, the IBM logic synthesis tool. Subsequently he managed IBM's logic synthesis group, and lead all of IBM's design automation research as the Senior Manager Design Automation at IBM Research from 1999-2004.

Leon has published over fifty papers on many aspects of high level, architectural and logic synthesis, low power design, placement driven synthesis and on the automatic placement and routing for schematic diagrams. He was elected an IEEE fellow for the development and application of high-level and logic synthesis algorithms. With a diverse background and a passion to develop efficient design platforms, he will be able to contribute strongly to the development and promotion of useful EDA standards.

Nomination Statement: IBM

The systems and products designed by IBM rely heavily on the ability to quickly and accurately design complex silicon functions. Over the last decades the silicon content of IBM systems has increased drastically. This requires a significant improvement in designer productivity. Something that can only be realized by design tools that are operating in flows that are as seamless as possible our design flows consist of a mixture of internally developed and externally acquired tools from most EDA vendors. The interoperability of this entire toolset is essential to deliver the productivity required. Therefore, IBM is a strong supporter of open EDA standards and technologies and vigorously supports the objectives of Si2.



Nominee: Intel

Representative: Rahul Goyal, Vice President, Global Supply Chain and Director, Research and Development Strategic Enablement



Rahul Goyal is vice president of the Global Supply Chain organization and director of Research and Development Strategic Enablement at Intel Corp. He has corporate-wide global responsibility for platform development and related strategic engagements with the industry ecosystem, strategic sourcing, supply chain strategy and innovation, industry relations, data analytics, and capacity management across Intel's broad product portfolio and strategic initiatives. This includes supporting revenue plans for business units across all market segments in collaboration with the ecosystem partners and supply base. His team is also responsible for sourcing and licensing software, semiconductor intellectual property, product development, engineering out sources services, electronic measurement solutions, electronic design automation products and services for product design, validation and technology development.

Goyal joined Intel in 1989 and has held various technical and management positions in software engineering and technology development. His previous roles include vice president of the EDA Business in Design and Technology Solutions Group, director of the integrated silicon technology road map in the Microprocessor Products Group and senior engineering manager in Intel Mask Operations.

Goyal represents Intel on the board of directors of Silicon Integration Initiative (Si2), an R&D collaborative industry consortium focused on design interoperability standards and adoption. He has served on the board of director of several private technology companies since 2000, and was chairman of the Design Technology Council, an industry think tank, from 2007-2009.

Before joining Intel, Goyal was a hardware design engineer

Nomination Statement: Intel

The systems and products designed by Intel Corporation rely heavily on the ability to quickly and accurately design complex silicon functions. Over the last ten years, not only has the silicon content of Intel systems increased exponentially, but a migration from a design environment of internally developed EDA tools to a large number of EDA tools acquired commercially has also occurred. Given that Intel subscribes to a multiple EDA vendor philosophy and uses a cross-section of tools from EDA vendors, the interoperability of those tools is essential for effective silicon design. Therefore, Intel is a strong supporter of open EDA standards and technologies and vigorously supports the objectives of Si2.

Nominee: Qualcomm Technologies

**Representative: Pankaj Kukkal, Vice President, EDA,
Emulation and Post-Silicon Engineering**

Pankaj Kukkal is vice president of Engineering at Qualcomm Inc. In his current role, he oversees all EDA, emulation and post-silicon engineering functions for mobile, compute, automotive, and artificial intelligence/machine learning business units. He joined Qualcomm in 2012 and has contributed to delivering over 50 leading-edge SoCs in various application domains. Pankaj has more than 25 years of experience in EDA, silicon, systems, and software engineering.



Before joining Qualcomm, he held various leadership positions at Intel, focusing on CAD, emulation and validation. He has led the creation of several industry-leading technologies for chip design, emulation and post-silicon debug and automation.

Pankaj has a bachelor's degree in electrical engineering from the National Institutes of Technology, India, and a master's degree in computer engineering from the University of South Carolina.

Pankaj has lived in South Carolina, Oregon, Texas and California. In his free moments he enjoys his time with his wife and two daughters. He also likes skiing and boogie boarding, and he can do both in and around San Diego!

Nomination Statement: Qualcomm Technologies

At Qualcomm, we invent breakthrough technologies that transform how the world connects, computes, and communicates. With a long-standing R&D focus, more than \$50 billion in cumulative research and development spend, over 130,000 patents and patent applications, and more than 30 years of innovation in chipsets, software, services and integrated platform solutions, we create foundational technologies that revolutionize the way people connect.

For decades, Qualcomm has helped enable the entire mobile ecosystem and powered many of your smartphone's capabilities. We were instrumental in driving the development and launch of 3G and 4G. Now, we're building upon that history of technology leadership as we do the same with 5G, which will have a significantly greater impact than previous generations. 5G serves as the foundational technology that makes it possible for everything and everyone to communicate and interact seamlessly, across connected cars and industrial IoT, smart homes and smart cities, networking and mobility. Qualcomm continues to break new ground, innovating across multiple technologies such as CPU, GPU, modem, GPS, connectivity, etc., and as a result is continually expanding our product offerings.

Nominee: Samsung Electronics

Representative: Dr. Jung Yun Choi, Corporate Vice President, Electronics Design Technology Team

Dr. Jung Yun Choi is corporate vice president for the Samsung Electronics Design Technology Team.

A 19-year Samsung veteran, Jung leads the design team responsible for developing all design tools and methodologies for Samsung memory products: technologies and environments impacting product values, new process and package technologies, new applications and new working environments such as the Cloud.

Since joining Samsung, he has contributed to the development of low-power design methodologies for mobile devices, RTL-to-GDS implementation and sign-off methodologies.

Jung joined Samsung Electronics in 2003 after receiving his doctorate in Electrical Engineering at the Pohang University of Science and Technology, Republic of Korea. He was also a visiting scholar at Stanford University in 2012.

Nomination Statement: Samsung Electronics

The Samsung Electronics Device Solutions Division has three semiconductor Business Groups: Memory Business, SLSI Business, and Foundry Business. We need to prepare a seamless design flow with diverse tools from different EDA vendors for not only internal designs (Memory and SLSI) but also outside customers (Foundry).



Nominee: Siemens Digital Industries Software

Representative: Juan C. Rey
Vice President of Engineering, Calibre

Juan C. Rey, vice president of Engineering, Calibre, joined Mentor in 2001 as senior engineering director for Mentor's industry-leading Calibre product line, directing all development activities for Calibre products.

Previously he was vice president of Engineering at Exend Corporation, managing all software development and quality activities. Prior to that he was engineering director for Physical Verification at Cadence Design Systems.

Earlier positions include: manager/developer for Process Modeling and Parasitic Extraction at Technology Modeling Associates; visiting scholar/science and engineering associate at Stanford University; senior research engineer at INVAP, Argentina; and associate professor at Universidad Nacional del Comahue, Argentina.

Juan holds a degree in Nuclear Engineering from Universidad Nacional de Cuyo, Argentina. The author or co-author of numerous papers and conference presentations, he serves on the Executive Technology Advisory Board of the Semiconductor Research Corporation and the UCLA Center for Domain-Specific Computing.



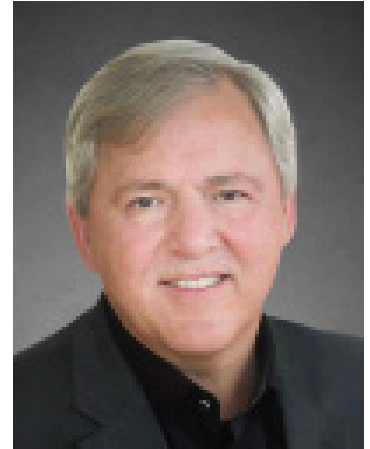
Nomination Statement: Siemens Digital Industries Software

Siemens Digital Industries Software is a world leader in electronic and software design solutions, providing products, consulting services, and award-winning support for the world's most successful electronic, semiconductor and systems companies. We are unique in providing solutions for both the hardware components (the chips and boards) and the software components (the embedded operations systems and applications/drivers that control the product's operation). Since its inception, the company has focused on providing leading tools for the design and verification of electronic systems with a focus on best-in-class solutions. Siemens Digital Industries Software strongly promotes open design flows that enable our customers to build flows combining best-in-class products. The interoperability of EDA tools and the support of open EDA standards have been central to this mission.

Nominee: **Silvaco Inc.**

Representative: Thomas F. Blaesi, Vice President and General Manager, EDA Business Unit

Thomas F. Blaesi is vice president and general manager of the EDA Business Unit at Silvaco. He is responsible for managing the development of all EDA tools including analog customer design, circuit simulation and SPICE modeling. Thomas joined Silvaco in October 2017 and held the position of vice president of Global Marketing until December 2019. He has more than 25 years of experience in corporate strategy, business development, and marketing in semiconductor, and electronic design automation industries. He has led major projects in SoC platform-based design, system-level design, and design for manufacturing in addition to hands-on experience in custom and semi-custom chip design and development.



Most recently, Thomas was the managing partner at Zeema Technologies. Before that, he served as CEO of Chipvision and held various senior business and technical positions at Cadence, Synopsys, and LSI Logic.

Thomas holds a BS in Electrical Engineering and Computer Science from Hochschule Furtwangen University, Germany.

Nomination Statement: Silvaco Inc.

As circuits become ever more complex and demanding on simulation, Silvaco is in a unique position to leverage a complete EDA software flow from basic foundry process steps to full device realization. Having this unique complete flow the company can explore novel device structures and materials to keep pace with a rapidly changing design environment. A key part of this Silvaco EDA flow is accurate simulation models. These device models can be derived from our TCAD data and measurement-based SPICE-extracted models. Therefore, Silvaco is a strong supporter and contributor to the evolution of standard device models to support the whole circuit design industry. With Si2 and CMC member contributions, designers have resources to enable them to explore new devices and circuits to strengthen the grow their companies and the whole industry benefits.

Nominee: SK-Hynix

**Representative: Do Chang-Ho, Vice President
Computer Aided Engineering Division**

Do Chang-ho has been the head of SK-Hynix's Computer Aided Engineering Division since December 2019. Prior to that, he was as vice president of Strategy & Planning in the DRAM Development Division. He majored in physics at Kyungpook National University in South Korea and graduated from his BA in 1996.

He started working in the design team of SK-Hynix Memory Research Center in 1996. He worked as a circuit design engineer for memory product development. From 2005 to 2013, he worked as a project leader in memory design. Started at 64M SDRAM development, contributing to the development of the world's first DDR3 product. He was also in charge of the organization dedicated to the development of Analog IP for Memory for a certain period of time. He was elected to the CEO office in 2013, and in 2016 he served as the team leader directly supporting the CEO of SK-Hynix.

Do Chang-ho was awarded the Industrial Service Medal from the Korean government in 2008 for his contributions to the industrial development of Korea. Currently, he holds more than 70 US patents related to the low power and high speed scheme, reliability and yield enhancement, and DFT/DFp in the field of memory design.

Nomination Statement: SK-Hynix

SK-Hynix is a leading semiconductor company that produces DRAM, NAND flash memory semiconductors and CIS non-memory semiconductor products, and has solidified its technological leadership by introducing innovative products with the world's first-minimum-fastest-lowest voltage to the market.

The emergence of new digital products and the expansion of the IoT environment are gradually expanding the area and demand of semiconductors, and the smartization and mobilization of IT devices demands more advanced semiconductor characteristics. To satisfy the characteristics of such advanced semiconductors, it is very important to design semiconductors quickly and accurately.

Semiconductor design requires the proper use of design tools provided by EDA vendors and internally developed (in-house) tools at each design stage, so compatibility between them is essential for efficient design. For this compatibility technology, SK-Hynix has adopted OA, the open EDA standard technology of Si2, and is continuously using and expanding it in internally developed tools. Therefore, SK-Hynix is actively supporting Si2's open EDA standards and technologies and is willing to provide leading support.



Nominee: Synopsys

**Representative: David DeMaria, Corporate Vice President,
Strategic Initiatives & Market Intelligence**

Dave DeMaria joined Synopsys in 2013 and is corporate vice president of Strategic Initiatives & Market Intelligence. He has more than 25 years of experience in the EDA, IP and semiconductor industries.

Prior to Synopsys, he held senior executive positions at Cadence, MoSys, Apache, Optimal, Viewlogic and Zuken. Dave attended Boston University for a B.S. degree in Computer Engineering.



Nomination Statement: Synopsys

Synopsys, Inc. provides products and services that accelerate innovation in the global electronics market. As a leader in EDA and semiconductor intellectual property (IP), Synopsys' comprehensive, integrated portfolio of system-level, IP, implementation, verification, manufacturing, optical and field-programmable gate array (FPGA) solutions help address the key challenges designers face such as power and yield management, system-to-silicon verification and time-to-results.

These technology-leading solutions help give Synopsys customers a competitive edge in quickly bringing the best products to market while reducing costs and schedule risk. For more than 30 years, Synopsys has been at the heart of accelerating electronics innovation with engineers around the world having used Synopsys technology to successfully design and create billions of chips and systems. The company is headquartered in Mountain View, California, and has approximately 90 offices located throughout North America, Europe, Japan, Asia and India.

Synopsys continues to champion customers' requirements for interoperability throughout the EDA and semiconductor industries. Synopsys has made strong and valuable contributions of technology, manpower, and funding to a variety of organizations and initiatives that have resulted in tangible benefits to the design community. Synopsys desires to continue its involvement with Si2 as a member of the Si2 Board of Directors to serve the electronics community by bringing expertise and resources to bear upon the ongoing challenge of interoperability for IC design and manufacturing. Synopsys agrees with Si2 that through collaborative efforts, the IC industry can achieve higher levels of SoC integration, improve productivity, and reduce cost.

Nominee: Texas Instruments

Representative: Keith Green, Distinguished Member of the Technical Staff

Dr. Keith Green is a Distinguished Member of the Technical Staff at Texas Instruments in Dallas, Texas. During his 28 years with TI he has had various technical and leadership roles that spanned the fields of semiconductor modeling, reliability and technology development. Presently, he works in TI's Analog Technology Development department and is responsible for Hall-effect magnetic sensor technology.

Keith was a founder of the Compact Model Council consortium in 1996 and served as its chairman from 2012 to 2015. He guided strategic university research as chairman of the Semiconductor Research Corporation's Compact Modeling Technical Advisory Board from 2004 to 2011. He has served on the board of Silicon Integration Initiative since 2015.

Dr. Green has 15 patents, over 20 publications, and has been an invited speaker at several conferences and universities. He received Ph.D. and M.S. degrees in Electrical Engineering from the University of Florida and a B.S. degree in Electrical Engineering from the University of Delaware.

Nomination Statement: Texas Instruments

Texas Instruments Incorporated (TI) is a global semiconductor design and manufacturing company that develops analog integrated circuits and embedded processors. The process of designing these products relies heavily on electronic design automation tools. The accuracy of these tools is as critical as their ability to operate reliably with technology design kits developed both in-house and by commercial foundries. Therefore, TI has a strong interest in the mission of Si2 to deliver standards for improving IC design capability. As an integrated device manufacturer, TI's interests span manufacturing, design, packaging and test. As a member of the board of directors, TI would bring perspective on all of these aspects for a wide spectrum of technologies that include silicon for low-power to high-voltage, gallium-nitride, MEMs and sensors.

