Si DAC Events 2026

Advancing Semiconductor Design

July 27th | Long Beach Convention Center | California

REGISTER

Don't forget to register for DAC separately!

Need pre-RTL power? Have more corners than you can afford? Test drive an IEEE 2416 Power Calculator!

Monday, July 27, 10:00 AM - 11:45 PM
Room 104C
REGISTER AND ATTEND TO BE ELIGIBLE FOR A PRIZE

Si2 OpenAccess Forum

Complimentary Lunch (first 50 attendees)
Monday, July 27, 12:00 PM - 1:00 pm
Room 104C
SESSION REGISTRATION

LLM Benchmarking for Chip Design – Live Demos and Strategic Outlook

Complimentary Lunch (first 50 attendees)
Monday, July 27, 1:00 PM - 2:30 PM
Room 104C
SESSION REGISTRATION

IEEE 2416 Working Group Meeting: Kickoff for Next Revision

Monday, July 27, 2:30 PM - 3:30 PM
Room 104C
SESSION REGISTRATION

Agentic AI in EDA: Who's in Control?

Monday, July 27, 4:00 PM - 4:45 PM
DAC Pavilion

Annual Si2 Member Meeting

Monday, July 27, 5:00 PM - 6:15 PM
Room 104C
SESSION REGISTRATION
Si2 Members and Guests

Learn more about us at www.si2.org

Need pre-RTL power? Have more corners than you can afford? Test drive an IEEE 2416 Power Calculator!

10:00 AM - 11:45 AM | ROOM 104C

Running PVT corner simulations today means higher cost, effort, and time; IEEE 2416 changes that by modelling pre-RTL/system-level and gate level power. You can build PVT independent power models once and use them to quickly analyze power across design phases, abstraction levels, and operating conditions.

Si2 has been working in tandem with IEEE 2416 for many years, proving out use cases with proof-of-concept code and demos. With the approval of IEEE 2416-2025, Si2 is proud to introduce the next generation of UPM PowerCalc, a new reference implementation for the standard.

This new power calculator has been written from the ground up with a focus on portability, modularity, and brevity. Utilizing mature, MIT licensed, open-source libraries has allowed the codebase to focus on the implementation of IEEE 2416 for power analysis.

In this workshop you will be introduced to IEEE 2416 and get hands-on with UPM PowerCalc in a demo environment. You will generate system-level power information for a provided sample design and be given several tasks of varying difficulty to help you understand and employ the IEEE power modelling standard.

What you will learn:

1. Highlights of IEEE 2416 and industry use cases
2. How to analyze power from architecture through implementation
3. Ways to calculate system-level power on real examples at multiple PVTs

Designed for architects planning systems, designers analyzing power, and everyone in between.

Be one of the first to see the standard in action!

Watch for Si2 DAC updates!

Speakers

Ali Sadigh | Si2

Dominic DeMarco | Si2

*Don't forget to register and attend to ensure you're eligible to enter a prize raffle

REGISTER

Si2 OpenAccess Forum

12:00 PM - 1:00 PM | ROOM 104C

Complimentary lunch provided for the first 50 attendees.

Come to the OpenAccess Forum 2026 and see what new EDA development is going on within the OpenAccess Coalition. We have several new members this year with some truly innovative ideas. The theme for DAC has been Artificial Intelligence for some time now and this year we expect to see more results from AI application.

Presentations will start at noon, we have lunch for the first fifty who attend.

Watch for Si2 DAC updates!

Moderator

Marshall Tiner | Si2

Speakers

Ma Yutao | Primarius **|** Application Driven Open Platform for Analog and Mixed Signal Design and Verification

Analog and mixed signal design and verification are facing bigger challenges due to increase design size and high accuracy requirement. A design platform based on OpenAccess and high efficiency, high flexibility design platform is essential to attack such challenges. Such a platform is presented in this talk with emphasizing on intelligent design flow, fast and accuracy verification solution as well as design signoff coverage including yield, ESD, EMIR and more.

Su Yi-Jen | Pulsaris AI **|** Introducing Pulsaris AI and Lyra: An AI-Native Layout Reshaping Agent

In advanced semiconductor design flows, convergence challenges around placement, routing, and downstream signoff remain a significant source of iteration cost. Pulsaris AI aims to apply multi-level optimization to reduce turnaround time and overall cost across the design flow. This presentation introduces Pulsaris AI and Lyra, an AI-native layout reshaping agent, and outlines key structural challenges observed in current physical design flows, Lyra's design approach and positioning, and early observations from applying the methodology in practice. Lyra supports LEF/DEF and OpenAccess.

Rakesh Kumar | Maieutic **|** GenAI Powered Circuit: Beyond Parametric Tuning: Generative AI for Analog Circuit Topology Exploration

Analog design automation has long been constrained by parametric optimizers with limited scope for topology exploration. Maieutic challenges this assumption with a generative AI framework that modifies circuit topologies during the optimization process — proposing device arrangements, not merely tuning within them — marking a step-function departure from decades of parametric optimizer-centric approaches. This shift introduces significant challenges: training data is scarce and proprietary, generated topologies must be PDK-aware and simulation-in-the-loop verification with good turnaround time. Realizing this promise at scale, however, requires that AI-generated design artifacts integrate seamlessly into existing flows — making the OpenAccess standard, stewarded by SI2, a critical enabler. All topology outputs from Maieutic's framework are expressed through OA-compliant interfaces, and we call on the SI2 community to ensure that the EDA ecosystem remains open and interoperable as AI-native design becomes mainstream.

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Speakers

Ed Gernert | Frontier Design **| Closing the IC Autorouting Feedback Loop with Large Language Models**

Hermes integrates Claude as an autonomous CI driver for Frontier, the next generation of shape-based interconnect tools. On every commit, Hermes runs the full routing regression suite, classifies failures, opens tickets. For regressions it cannot resolve and proposes — or directly applies — fixes for issues it can diagnose with confidence. The result is a tighter feedback loop: defects surface in minutes rather than days, first-pass repair. Happens without human intervention, and engineers stay focused on the harder algorithmic problems that resist automation. This talk covers the architecture, the failure modes we encountered handing autonomous agents. Full write access to a production codebase, and the measurable impact on engineering velocity.

Bobby Green | Astrus AI **:** The Ai agent for physics-aware chip design **| Scaling SerDes Subblock Layout: Automation for PLLs and Critical Analog Cells on State-of-the-Art Silicon**

PLLs and related analog subblocks within SerDes dominate layout effort and risk in many advanced SoCs. Astrus automates layout for this circuit class, with focus on advanced finFET and GAA processes at TSMC and Samsung. This session gives a concise overview of scope for analog designers and layout leads, and why automation matters for high-speed IO as technologies push deeper into advanced scaling regimes.

REGISTER

LLM Benchmarking for Chip Design – Live Demos and Strategic Outlook

1:00 PM - 2:30 PM | ROOM 104C

Complimentary lunch provided for the first 50 attendees.

The Si2 LLM Benchmarking Coalition is an effort under Silicon Integration Initiative (Si2) focused on advancing empirical evaluation for AI in chip design. At this special session the coalition members will present live demos and strategic outlook discussions.

The goal of the coalition is to bring together high-quality AI-for-chip design datasets into a consistent, reproducible format, operate a centralized leaderboard maintained by Si2 staff, and, as a community, establish reporting standards for how these benchmarks are used in the literature. More broadly, we aim to align the field around shared evaluation, improving benchmarks collaboratively rather than having them compete in isolation. You can find more details here: https://si2.org/llm-benchmarking-coalition/. We are also in the process of launching a public leaderboard to track model and agent performance, with a regular cadence of updates as datasets and methodologies evolve.
Presentations will start at 1:00 PM, we have lunch for the first fifty who attend.

Watch for Si2 DAC updates!

Moderators

Nathaniel Pinckney | Nvidia
Leigh Anne Clevenger | Si2

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IEEE 2416 Working Group Meeting: Kickoff for Next Revision

2:30 PM - 3:30 PM | ROOM 104C

Following the successful completion and publication of IEEE 2416-2025, which incorporates significant enhancements in multi-supply modeling, AMS extensions, and improved interoperability across abstraction levels, we will be initiating the next revision cycle of the standard through a new IEEE PAR. This effort is driven by ballot feedback, emerging use cases, and ongoing industry adoption needs around system-level power modeling and signoff integration. To kick off this next phase, we are organizing a one-hour face-to-face working group meeting at DAC, bringing together contributors from industry and academia to align on scope, technical direction, and key focus areas for the upcoming revision. This session is open to interested participants and is intended to foster collaboration and early engagement as we shape the future evolution of IEEE 2416.

Watch for Si2 DAC updates!

Speakers

Nagu Dhanwada | IBM, Chair, IEEE 2416 and IEEE 2416 Working Group members

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Agentic AI in EDA: Who's in Control?

4:00 PM - 4:45 PM | DAC PAVILION

EDA is on the brink of its most disruptive transformation yet. **Agentic AI**—multi-agent systems capable of autonomous, goal-driven decision-making—promises to move beyond assistive point solutions toward orchestrating entire design flows. From synthesis and verification to physical design and system optimization, these agents could redefine productivity and complexity management. Yet as autonomy grows, critical questions emerge: Who—or what—is really in control?

This panel will explore the technical, organizational, and ethical tensions surrounding agentic AI adoption. We'll examine **infrastructure and governance:** securing sensitive IP and maintaining compliance when autonomous agents operate across hybrid environments. We'll discuss **interoperability and standards**: for example, Si2's AI/ML EDA ontology provides a standardized representation of design terminology and relationships, bridging graph representations, ML datasets, and tool semantics to enable agents to reason about workflows. Such efforts highlight both the promise and the challenge of enabling multi-vendor collaboration without fragmenting the ecosystem. Finally, we'll confront **trust and accountability**: how do we reason about correctness, explainability, and oversight when design decisions emerge from interacting agents rather than deterministic scripts?

The discussion will surface points of disagreement across the ecosystem, including how much autonomy is desirable, which risks are acceptable, and whether current infrastructures and standards are sufficient. Attendees will leave with a clearer understanding of the readiness of agentic AI, practical tensions it raises, and open questions shaping its future adoption.

Agenda

1. Diverse industry perspectives on the promise and perils of agentic AI in EDA
2. Emerging standards and collaboration needs, including ontology-driven approaches, for interoperability
3. Critical risk areas—including security, governance, and trust—under debate
4. Points of contention and open questions shaping adoption strategies

Moderator

Leigh Anne Clevenger | Si2

Panelists

Natesan Venkateswaran | IBM

Ivan Kissiov | Siemens EDA

Lindsey Kostas | Qualcomm

Srinivas Bodapati | Samsung

Da Yang | Nvidia

Join Us at the Si2 Annual Member Celebration at DAC 2026

Monday, July 27th | 5:00 PM - 6:15 PM | Long Beach Convention Center Room 104C

Join us for a celebration of collaboration at our annual members' meeting and reception. Gather with members, the board of directors, staff, and special guests as we toast to our joint achievements over the past year and hear about new initiatives tasilored to address interoperability in the era of highly integrated systems and agentic AI. In the meeting, Si2 will also present the annual Power of Partnerships Award. The program will wrap up with a lively networking reception, where you can relax, connect, and share in the excitement with fellow DAC attendees.

Special Presentation

Si2's Growing Impact in the Age of AI - Robert Aslett **|** Si2 CEO and President

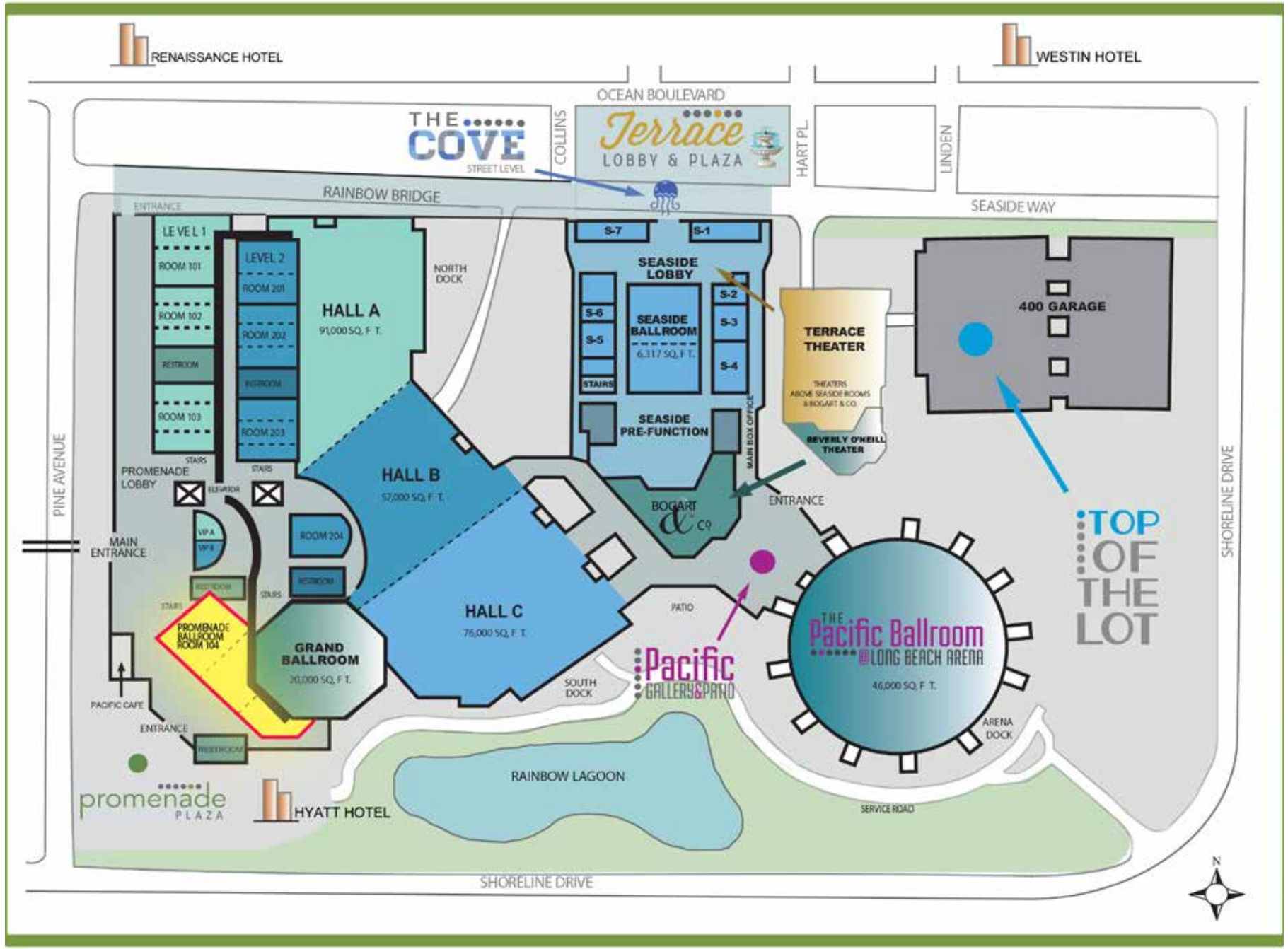
Presentation of Si2 Annual Power of Partnership (PoP) Award

Member Reception and Networking

Refreshments and more!

Admission is for Si2 members and their guests

REGISTER



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LOOKING FOR ANOTHER EVENT IN THE AREA?

ICMC 2026

International Compact Modeling Conference

July 30 - July 31, 2026 || The Queen Mary || Long Beach, CA

The Compact Model Coalition (CMC) brings academia and industry partners together in the development and standardization of compact models for semiconductor devices. For 30 years now, the CMC has been instrumental in creating standardized and verified models for designers to use in their increasingly complex circuits for SPICE simulation.

Keynote Speakers

Prof. Dr. Chenming Hu
TSMC Distinguished Chair
Professor Emeritus, University of California, Berkeley

Prof. Dr. Elyse Rosenbaum
University of Illinois Urbana-Champaign

Prof. Dr. Yuan Taur
University of California, San Diego

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